ACT8870 Register Definitions – CMI 101

Abstract

This application note identifies and explains the ACT8870 internal registers that help make this IC flexible and configurable for many applications. It provides a short description of each register, its individual bits, their function, and default values. This application note is specific to the Code Matrix Index, CMI 101.

Introduction

The ACT8870 is an ActivePMU power management unit from Active-Semi. It is designed to power a wide range of processors, FPGA's, peripherals, microcontroller and solid-state drive applications. The ACT8870 core includes 4 DC/DC step down converters using integrated power FETs and 3 low-dropout regulators (LDOs). Each regulator can be configured for a wide range of output voltages through the I2C interface.

Today's processors require more complexity in their startup and sequencing requirements. This is also true for entering and exiting sleep and low power modes. The ACT8870 is specifically designed to meet today's processors' stringent power system requirements. These processors include, but are not limited to

Atmel SAMA5D, SAMA9G

Rockchip RK2906, RK2918

Samsung S3C2416, S3C2440, S3C2450

Core Logic

Although the ACT8870 is programmed at the factory with a default configuration, these settings can be changed through the I2C interface to provide customized configurations optimized for a specific processor and/or end application. IC configurability includes many options such as output voltage, startup sequencing, startup timing, slew rates, GPIO configuration, fault responses, and more. Active-Semi identifies these configurations with a Code Matrix Index, CMI. An IC's CMI is identified by the last three digits at the end of the orderable part number. Note that this application note is specific to the ACT8870's CMI 101. Refer to the appropriate application note for register information for other CMI versions.

Register Types

The ACT8870 contains the following register types.

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

The ACT8870 contains seven major register spaces.

Master Reg	0x00h to 0x2Fh
Buck1 Reg	0x30h to 0x3Fh
Buck2 Reg	0x40h to 0x4Fh
Buck3 Reg	0x50h to 0x5Fh
Buck4 Reg	0x60h to 0x6Fh
LDO1 Reg	0x70h thru 0x7Fh
LDO23 Reg	0x80h thru 0x8Fh

MASTER REGISTERS

MSTR00 - Master Configuration Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	nRST_AUX1_MASK	nRST_AUX2_MASK	nRST_MASK	RFU	POK_nMASK	IRQ_nMASK	DVS_EN	PWRDN_EN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
nRST_AUX1_MASK	0 - Masks nRESET_AUX1 output 1 - Unmasks nRESET _AUX1 output	When masked, nRESET_AUX1 will not be asserted low when its associated power supplies drop out of regulation.
nRST_AUX2_MASK	0 - Masks nRESET _AUX2 output 1 - Unmasks nRESET _AUX2 output	When masked, nRESET_AUX2 will not be asserted low when its associated power supplies drop out of regulation.
nRST_MASK	0 - Masks nRESET output 1 - Unmasks nRESET output	When masked, nRESET will not be asserted low when its associated power supplies drop out of regulation.
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
POK_nMASK	0 - Masks POK output 1 - Unmasks POK output	
IRQ_nMASK	0 - Masks IRQ output 1 – Unmasks IRQ output	
DVS_EN	0 - Disables dynamic voltage scaling 1 - Enables dynamic voltage scaling	Regardless of the DVS_EN setting, DVS is always enabled in CMI 101. Typically, DVS_EN is required to enable DVS mode. When DVS_EN=1 the buck converters can enter DVS mode when the EXT_PG goes high.
PWRDN_EN	0 – Prevents SLP_ENTR and the PWREN pin from putting the IC into Sleep mode. 1 – Enables Sleep mode.	This is a global bit that prevents any input from putting the IC into Sleep mode. This bit is not used in CMI 101.

MSTR01 - Master Configuration Register

Address = 0x01h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[5:0]						SLP_ENTR	IDLE_ENTR
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[5:0]	Reserved for future use	Can write to this register, but it always returns a 0 when read.
SLP_ENTR	0 – normal operation 1 – Puts the IC into Sleep mode	This bit must be enabled by PWR_DN_MODE and PWR_DN_EN. SLEEP mode is not available in CMI 101.
IDLE_ENTR	0 – normal operation 1 – Puts the IC into Idle mode	

MSTR02 - Master Configuration Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	CURRENT_STATE[2:0]			PWREN_STAT	TSD_SHUTDWN	TSD_ALERT	POK_OV	POK_UV
Default	000			0	0	0	0	0
Access	RO			RO	RO	RO	RO	RO

Name	Description	Notes
CURRENT_STATE[2:0]	000=RESET - Info only 001=ACTIVE 010=SLEEP – Info only 100=THERMAL - Info only 101=OVUVFLT - Info only	Provides the current state of the ACT8870 internal state machine. Note that the register can only be read when the IC is in ACTIVE mode.
PWREN_STAT	0 – PWREN pin is not asserted 1 – PWREN pin is asserted	Internal status of PWREN pin after the polarity from PWREN_POL is applied.
TSD_SHUTDWN	0 – IC temperature is below the thermal shutdown temperature 1 – IC temperature is above the thermal shutdown temperature	If TSD_nMASK = 0, it provides real time status of overtemperature fault status. If TSD_nMASK = 1, it latches a 1 when overtemperature is exceeded until the bit is read via I2C.
TSD_ALERT	0 – IC temperature is below the thermal warn temperature 1 – IC temperature is above the thermal warn temperature	If IRQ_nMASK = 0, it provides real time status of the temperature warn. If IRQ_nMASK = 1, it latches a 1 when an overtemperature warn is exceeded until the bit is read via I2C.
POK_OV	0 – VIN voltage is below the POK_OV threshold 1 - VIN voltage is above the POK_OV threshold	If POK_nMASK = 0, it provides real-time status of POK_OV. If POK_nMASK = 1, it latches a 1 when POK_OV is tripped until the bit is read via I2C.
POK_UV	0 – VIN voltage is above the POK_UV threshold 1 - VIN voltage is below the POK_UV threshold	If POK_nMASK = 0, it provides real-time status of POK_OV. If POK_nMASK = 1, it latches a 1 when POK_UV is tripped until the bit is read via I2C.

MSTR03 - Master Configuration Register

Address = 0x03h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[5:0]						GPIO_STAT	MODE_STAT
Default	000000						0	0
Access	RO						R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
GPIO_STAT	0 – GPIO pin is a logic low 1 – GPIO pin is a logic high	
MODE_STAT	0 – MODE pin is a logic low 1 – MODE pin is a logic high	

MSTR04 - Master Configuration Register

Address = 0x04h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	ILIM_REG[6]	ILIM_REG[5]	ILIM_REG[4]	ILIM_REG[3]	ILIM_REG[2]	ILIM_REG[1]	ILIM_REG[0]
Default	0	0	0	0	0	0	0	0
Access	R/W	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
ILIM_REG[6]	0 - LDO3 not detected current limit. 1 - LDO3 detected current limit. Asserts IRQ	This is the latched version of LDO3_ILIM overcurrent threshold. Overcurrent threshold set by LDO3_ILIM. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[5]	0 – LDO2 not detected current limit. 1 – LDO2 detected current limit. Asserts IRQ	This is the latched version of LDO2_ILIM overcurrent threshold. Overcurrent threshold set by LDO2_ILIM. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[4]	0 – LDO1 not detected current limit. 1 – LDO1 detected current limit. Asserts IRQ	This is the latched version of LDO1_ILIM overcurrent threshold. Overcurrent threshold set by LDO1_ILIM. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[3]	0 – Buck4 not detected current limit. 1 – Buck4 detected current limit. Asserts IRQ	This is the latched version of BUCK4_ILIM overcurrent threshold. Overcurrent threshold set by BUCK4_ILIM. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[2]	0 – Buck3 not detected current limit. 1 – Buck3 detected current limit. Asserts IRQ	This is the latched version of BUCK3_ILIM overcurrent threshold. Overcurrent threshold set by BUCK3_ILIM. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[1]	0 – Buck2 not detected current limit. 1 – Buck2 detected current limit. Asserts IRQ	This is the latched version of BUCK2_ILIM overcurrent threshold. Overcurrent threshold set by BUCK2_ILIM. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[0]	0 – Buck1 not detected current limit. 1 – Buck1 detected current limit. Asserts IRQ	This is the latched version of BUCK1_ILIM overcurrent threshold. Overcurrent threshold set by BUCK1_ILIM. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.

MSTR05 - Master Configuration Register

Address = 0x05h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	OV_REG[6]	OV_REG[5]	OV_REG[4]	OV_REG[3]	OV_REG[2]	OV_REG[1]	OV_REG[0]
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
OV_REG[6]	0 - LDO3 not detected overvoltage. 1 - LDO3 detected overvoltage. Asserts IRQ	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[5]	0 – LDO2 not detected overvoltage. 1 – LDO2 detected overvoltage. Asserts IRQ	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[4]	0 – LDO1 not detected overvoltage. 1 – LDO1 detected overvoltage. Asserts IRQ	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[3]	0 – Buck4 not detected overvoltage. 1 – Buck4 detected overvoltage. Asserts IRQ	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[2]	0 – Buck3 not detected overvoltage. 1 – Buck3 detected overvoltage. Asserts IRQ	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[1]	0 – Buck2 not detected overvoltage. 1 – Buck2 detected overvoltage. Asserts IRQ	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[0]	0 – Buck1 not detected overvoltage. 1 – Buck1 detected overvoltage. Asserts IRQ	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.

MSTR06 - Master Configuration Register

Address = 0x06h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	UV_REG[6]	UV_REG[5]	UV_REG[4]	UV_REG[3]	UV_REG[2]	UV_REG[1]	UV_REG[0]
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
UV_REG[6]	0 - LDO3 not detected undervoltage. 1 - LDO3 detected undervoltage. Asserts IRQ	This is the inverted LDO3_PWR_GOOD signal. Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. This bit is latched until read via I2C.
UV_REG[5]	0 – LDO2 not detected undervoltage. 1 – LDO2 detected undervoltage. Asserts IRQ	This is the inverted LDO2_PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[4]	0 – LDO1 not detected undervoltage. 1 – LDO1 detected undervoltage. Asserts IRQ	This is the inverted LDO1_PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[3]	0 – Buck4 not detected undervoltage. 1 – Buck4 detected undervoltage. Asserts IRQ	This is the inverted BUCK4_PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[2]	0 – Buck3 not detected undervoltage. 1 – Buck3 detected undervoltage. Asserts IRQ	This is the inverted BUCK3_PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[1]	0 – Buck2 not detected undervoltage. 1 – Buck2 detected undervoltage. Asserts IRQ	This is the inverted BUCK2_PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[0]	0 – Buck1 not detected undervoltage. 1 – Buck1 detected undervoltage. Asserts IRQ	This is the inverted BUCK1_PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.

MSTR07 - Master Configuration Register

Address = 0x07h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	"Reserved for factory use only"							
Default	"Reserved for factory use only"							
Access	N/A							

Name	Description	Notes
N/A	Reserved for factory use	Do not write to this register. Reading this register returns 0x00h

MSTR08 - Master Configuration Register

Address = 0x08h	Default = 0xE8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	nRST_DLY[2:0]			POK_UV_SET[1:0]		EXT_EN_POL	PWR_DN_MODE	PWR_DN_POL
Default	111			01		0	0	0
Access	R/W			R/W		R/W	R/W	R/W

Name	Description		Notes
nRST_DLY[2:0]	000 = 199us 001 = 313us 010 = 427us 011 = 540us 100 = 654us 101 = 768us 110 = 882us 111 = 996us		Sets the nRESET delay time.
POK_UV_SET[1:0]	VIN_LVL=0 00 = 88% of 3.3V (2.90V) 01 = 86% of 3.3V (2.84V) 10 = 84% of 3.3V (2.77V) 11 = Disable POK_UV	VIN_LVL=1 00 = 88% of 3.3V (2.90V) 01 = 85% of 3.3V (2.80V) 10 = 85% of 5.0V (4.25V) 11 = Disable POK_UV	Sets the POK_UV threshold. The VIN_LVL bit determines which table POK_UV uses. VIN_LVL is in a Factory register and is not user accessible. VIN_LVL = 1 for CMI 101
EXT_EN_POL	0 – Sets EXT_EN polarity to active high 1 – Sets EXT_EN polarity to active low		
PWR_DN_MODE	0 – Enables putting IC into Sleep mode via the PWREN pin 1 – Enables putting IC into Sleep mode via SLP_ENTR register		Sleep mode is disabled in CMI 101. Changing the value of this bit may result in unexpected IC behavior.
PWR_DN_POL	0 – Sets polarity of PWREN pin to active high 1 – Sets polarity of PWREN pin to active low		

MSTR09 - Master Configuration Register

Address = 0x09h	Default = 0x37h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK_OV_SET[1:0]		nRESET_AUX1_DLY[2:0]]			nRESET_AUX2_DLY[2:0]		
Default	00		110			111		
Access	R/W		R/W			R/W		

Name	Description			Notes
	VIN_LVL=0	VIN_LVL=1, POK_LVL=0	VIN_LVL=1, POK_LVL=1	
POK_OV_SET[1:0]	00 = 107% of 3.3V (3.53V) 01 = 109% of 3.3V (3.60V) 10 = 110% of 3.3V (3.69V) 11 = Disable POK_OV	00 = 133% of 3.3V (4.40V) 01 = 136% of 3.3V (4.50V) 10 = 136% of 3.3V (4.50V) 11 = Disable POK_OV	00 = 110% of 5V (5.50V) 01 = 112% of 5V (5.60V) 10 = 114% of 5V (5.70V) 11 = Disable POK_OV	Sets the POK_OV threshold. The VIN_LVL and POK_LVL bits determine which table POK_OV uses. Both VIN_LVL and POK_LVO are in Factory registers and are not user accessible. VIN_LVL = 1 for CMI 101. POL_LVL= 0 for CMI 101.
nRESET_AUX1_DLY[2:0]	000 = 398us 001 = 626us 010 = 853us 011 = 1081us 100 = 1308us 101 = 1536us 110 = 1764us 111 = 1991us			Sets the nRESET_AUX1 delay time.
nRESET_AUX2_DLY[2:0]	000 = 199us 001 = 313us 010 = 427us 011 = 540us 100 = 654us 101 = 768us 110 = 882us 111 = 996us			Sets the nRESET_AUX2 delay time.

MSTR0A - Master Configuration Register

Address = 0x0Ah	Default = 0x1Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	GPIO_OUT	VIN_OV_MASK	TSD_nMASK	UV_nMASK	OV_nMASK	RFU	EXT_PG_POL
Default	0	0	0	1	1	1	0	0
Access	RO	R/W	R/W	R/W	R/W	R/W	RO	R/W

Name	Description	Notes
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
GPIO_OUT	0 – Forces the GPIO pin to high impedance 1 – Forces the GPIO pin to ground (logic 0)	Must be set to 0 to use the GPIO as an input
VIN_OV_MASK	0 – Unmasks the POK_OV 1 – Masks the POK_OV	If VIN_OV_MASK=0 then system enters the RESET state with an input voltage OV condition. If VIN_OV_MASK=1, the system ignores input overvoltage and continue to operate in ACTIVE state
TSD_nMASK	0 – Prevents the IC from entering the THERMAL state 1 – Allows the IC to enter the THERMAL state	When low, it prevents thermal shutdown, but still allows the TSD_SHUTDWN bit in register MSTR02 to provide the real-time overtemperature status. When high, it allows thermal shutdown and causes TSD_SHUTDWN to latch the overtemperature event until the bit is read via I2C.
UV_nMASK	0 – Masks an undervoltage condition from allowing the IC to enter the UVOVFLT state. 1 – Unmasks an undervoltage condition from allowing the IC to enter the UVOVFLT state.	When 1, this register allows the IC to enter the UVOVFLT state when any regulator enters an undervoltage condition.
OV_nMASK	0 – Masks an overvoltage condition from allowing the IC to enter the UVOVFLT state. 1 – Unmasks an overvoltage condition from allowing the IC to enter the UVOVFLT state.	When 1, this register allows the IC to enter the UVOVFLT state when any regulator enters an overvoltage condition.
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
EXT_PG_POL	0 – Sets EXT_PG polarity to active high 1 – Sets EXT_PG polarity to active low	The polarity functionality is only valid when EXT_PG is configured as an input by pulling the MODE pin high. This function is disabled in CMI 101.

BUCK REGULATORS REGISTERS

Buck1 Registers

B1_REG00 – Buck1 Configuration Register

Address = 0x30h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	B1_PWR_GOOD	B1_OV	B1_ILIM	RFU	B1_nRESET_FLTMSK	B1_ILIM_FLTMSK	B1_UV_FLTMSK	B1_OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
B1_PWR_GOOD	0 - Buck1 voltage is below the power good threshold 1 – Buck1 voltage is above the power good threshold	Provides real-time power good status
B1_OV	0 - Buck1 voltage is above the overvoltage threshold 1 – Buck1 voltage is below the overvoltage threshold	Provides real-time overvoltage status
B1_ILIM	0 - Buck1 is below the ILIM threshold 1 – Buck1 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
B1_nRESET_FLT_MSK	0 - Unmasks the Buck1 POK signal 1 - Masks the Buck1 POK signal	When 1, the Buck1 POK signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nRESET pin when it is disabled or drops out of regulation.
B1_ILIM_FLTMSK	0 - Unmasks the Buck1 B1_ILIM register 1 - Masks the Buck1 B1_ILIM register	When 1, the B1_ILIM fault bit is masked from the master ILIM fault register, MSTR04. B1_ILIM still provides real-time current limit status.
B1_UV_FLTMSK	0 - Unmasks the Buck1 B1_UV register 1 - Masks the Buck1 B1_UV register	When 1, the B1_UV fault bit is masked from the master UV fault register, MSTR06. B1_UV still provides real-time current limit status.
B1_OV_FLTMSK	0 - Unmasks the Buck1 B1_OV register 1 - Masks the Buck1 B1_OV register	When 1, the B1_OV fault bit is masked from the master OV fault register, MSTR05. B1_OV still provides real-time overvoltage status.

B1_VSET00 – Buck1 Voltage Set0 Register

Address = 0x31h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B1_VSET0[7:0]							
Default	00001000							
Access	R/W							

Name	Description	Notes
B1_VSET0[7:0]	Buck1 output voltage setting in ACTIVE mode.	Controls the Buck1 output voltage. B1_VSET0 is used in ACTIVE mode. The output voltage is equal to B1_VSET * 0.0125 + 0.8V

B1_VSET01 – Buck1 Voltage Set1 Register

Address = 0x32h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B1_VSET1[7:0]							
Default	00001000							
Access	R/W							

Name	Description	Notes
B1_VSET1[7:0]	Buck1 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck1 output voltage. B1_VSET1 is used in DVS or SLEEP modes. The output voltage is equal to B1_VSET * 0.0125 + 0.8V

B1_REG03 – Buck1 Configuration Register

Address = 0x33h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_RAMP[2:0]		
Default	0	0	0	0	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON	0 – Buck1 is enabled through normal sequencing 1 – Buck1 is enabled via I2C that bypasses normal sequencing	
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck1 shuts down when its sequenced input shuts down 1 – Buck1 stays on when its sequenced input shuts down	
SLEEPEN	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	
DREN	0 - Unmasks the Buck1 POK signal 1 - Masks the Buck1 POK signal	When 1, the Buck1 POK signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nRESET pin when it is disabled or drops out of regulation.
SS_RAMP[2:0]	000 = 300us 001 = 400us 010 = 500us 011 = 600us 100 = 700us 101 = 800us 110 = 000us 111 = 1000us	Buck1 softstart ramp timing.

B1_REG04 – Buck1 Configuration Register

Address = 0x34h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	0	0	001			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck1 does not affect nRESET_AUX1 output 1 – Buck1 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG05 – Buck1 Configuration Register

Address = 0x35h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
Default	0000				10		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SLEW[1:0]	00 = not allowed 01 = 14mV/us 10 = 3.5mV/us 11 = 0.88mV/us	Sets Buck1 slew rate when changing between VSET0 and VSET1 voltages. During the transition between voltages, PWR_GOOD, OV, and ILIM are automatically masked to avoid nRESET assertion. Setting to 00 is not allowed.
DBSTBY[1:0]	Determines sleep mode inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG06 – Buck1 Configuration Register

Address = 0x36h	Default = 0x1Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	DISLPM	ONDLY[2:0]			DRVADJ[1:0]	
Default	0	0	0	111			11	
Access	R/W	R/W	R/W	R/W			R/W	

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	The PHASE bit aligns the converter switching to the rising or falling clock edge.
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	The PHASE_DELAY bit aligns the converter switching to the clock edge or to a 100ns delay from the clock edge.
DISLPM	0 – Low Power Mode enabled 1 – Low Power Mode disabled	
ONDLY[2:0]	000 34.5µs 001 106.5 µs 010 206.5 µs 011 306.5 µs 100 406.5 µs 101 506.5 µs 110 606.5 µs 111 706.5 µs	Programs the delay time between the Buck1 input trigger and when it turns on.
DRVADJ[1:0]	00 = 6.3ns rise time, 9.0ns fall time 01 = 4.5ns rise time, 7.4ns fall time 10 = 3.1ns rise time, 5.9ns fall time 11 = 3.0ns rise time, 5.0ns fall time	Sets the Buck1 switching rise and fall times. Faster rise times give higher efficiency while slower times give lower noise and EMI. These times change with Vin, load current, inductor value, etc and are intended to provide relative timing between settings.

B1_REG07 – Buck1 Configuration Register

Address = 0x37h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	"Reserved for factory use only"							
Default	"Reserved for factory use only"							
Access	N/A							

Name	Description	Notes
N/A	Reserved for factory use	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

BUCK2 REGISTERS

Note: Buck2, Buck3, Buck4 have the same registers but the default register values may be different

B2_REG00 – Buck2 Configuration Register

Buck2 Address = 0x40h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	B2_PWR_GOOD	B2_OV	B2_ILIM	RFU	RFU	B2_ILIM_FLTMSK	B2_UV_FLTMSK	B2_OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
B2_PWR_GOOD	0 – Buck2 voltage is below the power good threshold 1 – Buck2 voltage is above the power good threshold	Provides real-time power good status
B2_OV	0 – Buck2 voltage is above the overvoltage threshold 1 – Buck2 voltage is below the overvoltage threshold	Provides real-time overvoltage status
B2_ILIM	0 – Buck2 is below the ILIM threshold 1 – Buck2 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
B2_ILIM_FLTMSK	0 - Unmasks the Buck2 B2_ILIM register 1 - Masks the Buck2 B2_ILIM register	When 1, the B2_ILIM fault bit is masked from the master ILIM fault register, MSTR04. B2_ILIM still provides real-time current limit status.
B2_UV_FLTMSK	0 - Unmasks the Buck2 B2_UV register 1 - Masks the Buck2 B2_UV register	When 1, the B2_UV fault bit is masked from the master UV fault register, MSTR06. B2_UV still provides real-time current limit status.
B2_OV_FLTMSK	0 - Unmasks the Buck2 B2_OV register 1 - Masks the Buck2 B2_OV register	When 1, the B2_OV fault bit is masked from the master OV fault register, MSTR05. B2_OV still provides real-time overvoltage status.

B2_VSET00 – Buck2 Voltage Set0 Register

Buck2 Address = 0x41h	Default = 0x38h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B1_VSET0[7:0]							
Default	00111000							
Access	R/W							

Name	Description	Notes
B2_VSET0[7:0]	Buck2 output voltage setting in ACTIVE mode.	Controls the Buck2 output voltage. B2_VSET0 is used in ACTIVE mode. The output voltage is equal to B2_VSET0 * 0.0125 + 0.8V

B2_VSET01 – Buck2 Voltage Set1 Register

Address = 0x42h	Default = 0x2Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B2_VSET1[7:0]							
Default	00101100							
Access	R/W							

Name	Description	Notes
B2_VSET1[7:0]	Buck2 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck2 output voltage. B2_VSET1 is used in DVS or SLEEP modes. The output voltage is equal to B2_VSET1 * 0.0125 + 0.8V

B2_REG03 – Buck2 Configuration Register

Address = 0x43h	Default = 0xC2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_RAMP[2:0]		
Default	1	1	0	0	0	010		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON	0 – Buck2 is enabled through normal sequencing 1 – Buck2 is enabled via I2C that bypasses normal sequencing	
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck2 shuts down when its sequenced input shuts down 1 – Buck2 stays on when its sequenced input shuts down	
SLEEPEN	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	
DREN	0 - Unmasks the Buck2 POK signal 1 - Masks the Buck2 POK signal	When 1, the Buck2 POK signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nRESET pin when it is disabled or drops out of regulation.
SS_RAMP[2:0]	000 = 300us 001 = 400us 010 = 500us 011 = 600us 100 = 700us 101 = 800us 110 = 000us 111 = 1000us	Buck2 softstart ramp timing.

B2_REG04 – Buck2 Configuration Register

Address = 0x44h	Default = 0xDCh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	1	001			100		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck2 does not affect nRESET_AUX1 output 1 – Buck2 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B2_REG05 – Buck2 Configuration Register

Address = 0x45h	Default = 0x09h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
Default	0000				10		01	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SLEW[1:0]	00 = not allowed 01 = 14mV/us 10 = 3.5mV/us 11 = 0.88mV/us	Sets Buck2 slew rate when changing between VSET0 and VSET1 voltages. During the transition between voltages, PWR_GOOD, OV, and ILIM are automatically masked to avoid nRESET assertion. Setting to 00 is not allowed.
DBSTBY[1:0]	Determines sleep mode inputs from the CMI code	Sets Buck1 slew rate when changing between VSET0 and VSET1 voltages. During the transition between voltages, PWR_GOOD, OV, and ILIM are automatically masked to avoid nRESET assertion. Setting to 00 is not allowed.

B2_REG06 – Buck2 Configuration Register

Address = 0x46h	Default = 0x4Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	DISLPM	ONDLY[2:0]			DRVADJ[1:0]	
Default	0	1	0	010			10	
Access	R/W	R/W	R/W	R/W			R/W	

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	The PHASE bit aligns the converter switching to the rising or falling clock edge.
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	The PHASE_DELAY bit aligns the converter switching to the clock edge or to a 100ns delay from the clock edge.
DISLPM	0 – Low Power Mode enabled 1 – Low Power Mode disabled	
ONDLY[2:0]	000 34.5µs 001 106.5 µs 010 206.5 µs 011 306.5 µs 100 406.5 µs 101 506.5 µs 110 606.5 µs 111 706.5 µs	Programs the delay time between the Buck2 input trigger and when it turns on.
DRVADJ[1:0]	00 = 6.3ns rise time, 9.0ns fall time 01 = 4.5ns rise time, 7.4ns fall time 10 = 3.1ns rise time, 5.9ns fall time 11 = 3.0ns rise time, 5.0ns fall time	Sets the Buck2 switching rise and fall times. Faster rise time give higher efficiency while slower times give lower noise and EMI. These times change with Vin, load current, inductor value, etc and are intended to provide relative timing between settings.

B2_REG07 – Buck2 Configuration Register

Address = 0x47h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	"Reserved for factory use only"							
Default	"Reserved for factory use only"							
Access	N/A							

Name	Description	Notes
N/A	Reserved for factory use	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

BUCK3 REGISTERS

B3_REG00 – Buck3 Configuration Register

Buck3 Address = 0x50h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	B3_PWR_GOOD	B3_OV	B3_ILIM	RFU	RFU	B3_ILIM_FLTMSK	B3_UV_FLTMSK	B3_OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
B3_PWR_GOOD	0 – Buck3 voltage is below the power good threshold 1 – Buck3 voltage is above the power good threshold	Provides real-time power good status
B3_OV	0 – Buck3 voltage is above the overvoltage threshold 1 – Buck3voltage is below the overvoltage threshold	Provides real-time overvoltage status
B3_ILIM	0 – Buck3 is below the ILIM threshold 1 – Buck3 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
B3_ILIM_FLTMSK	0 - Unmasks the Buck3 B3_ILIM register 1 - Masks the Buck3 B3_ILIM register	When 1, the B3_ILIM fault bit is masked from the master ILIM fault register, MSTR04. B3_ILIM still provides real-time current limit status.
B3_UV_FLTMSK	0 - Unmasks the Buck3 B3_UV register 1 - Masks the Buck3 B3_UV register	When 1, the B3_UV fault bit is masked from the master UV fault register, MSTR06. B3_UV still provides real-time current limit status.
B3_OV_FLTMSK	0 - Unmasks the Buck3 B3_OV register 1 - Masks the Buck3 B3_OV register	When 1, the B3_OV fault bit is masked from the master OV fault register, MSTR05. B3_OV still provides real-time overvoltage status.

B3_VSET00 – Buck3 Voltage Set0 Register

Buck3 Address = 0x51h	Default = 0x24h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B3_VSET0[7:0]							
Default	00100100							
Access	R/W							

Name	Description	Notes
B3_VSET0[7:0]	Buck3 output voltage setting in ACTIVE mode.	Controls the Buck3 output voltage. B3_VSET0 is used in ACTIVE mode. The output voltage is equal to B3_VSET0 * 0.0125 + 0.8V

B3_VSET01 – Buck3 Voltage Set1 Register

Address = 0x52h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B3_VSET1[7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
B3_VSET1[7:0]	Buck3 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck3 output voltage. B3_VSET1 is used in DVS or SLEEP modes. The output voltage is equal to B3_VSET * 0.0125 + 0.8V

B3_REG03 – Buck3 Configuration Register

Address = 0x53h	Default = 0xC4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_RAMP[2:0]		
Default	1	1	0	0	0	100		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON	0 – Buck3 is enabled through normal sequencing routing 1 – Buck3 I2C enable that bypasses normal sequencing	
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck3 shuts down when its sequenced input shuts down 1 – Buck3 stays on when its sequenced input shuts down	
SLEEPEN	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	
DREN	0 - Unmasks the Buck3 POK signal 1 - Masks the Buck3 POK signal	When 1, the Buck3 POK signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nRESET pin when it is disabled or drops out of regulation.
SS_RAMP[2:0]	000 = 300us 001 = 400us 010 = 500us 011 = 600us 100 = 700us 101 = 800us 110 = 000us 111 = 1000us	Buck3 softstart ramp timing.

B3_REG04 – Buck3 Configuration Register

Address = 0x54h	Default = 0xA0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	100			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck3 does not affect nRESET_AUX1 output 1 – Buck3 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B3_REG05 – Buck3 Configuration Register

Address = 0x55h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
Default	0000				10		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SLEW[1:0]	00 = not allowed 01 = 14mV/us 10 = 3.5mV/us 11 = 0.88mV/us	Sets Buck3 slew rate when changing between VSET0 and VSET1 voltages. During the transition between voltages, PWR_GOOD, OV, and ILIM are automatically masked to avoid nRESET assertion. Setting to 00 is not allowed.
DBSTBY[1:0]	Determines sleep mode inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B3_REG06 – Buck3 Configuration Register

Address = 0x56h	Default = 0x9Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	DISLPM	ONDLY[3:0]			DRVADJ[1:0]	
Default	1	0	0	111			10	
Access	R/W	R/W	R/W	R/W			R/W	

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	The PHASE bit aligns the converter switching to the rising or falling clock edge.
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	The PHASE_DELAY bit aligns the converter switching to the clock edge or to a 100ns delay from the clock edge.
DISLPM	0 – Low Power Mode enabled 1 – Low Power Mode disabled	
ONDLY[3:0]	000 34.5µs 001 106.5 µs 010 206.5 µs 011 306.5 µs 100 406.5 µs 101 506.5 µs 110 606.5 µs 111 706.5 µs	Programs the delay time between the Buck3 input trigger and when it turns on.
DRVADJ[1:0]	00 = 6.3ns rise time, 9.0ns fall time 01 = 4.5ns rise time, 7.4ns fall time 10 = 3.1ns rise time, 5.9ns fall time 11 = 3.0ns rise time, 5.0ns fall time	Sets the Buck3 switching rise and fall times. Faster rise time give higher efficiency while slower times give lower noise and EMI. These times change with Vin, load current, inductor value, etc and are intended to provide relative timing between settings.

B3_REG07 – Buck3 Configuration Register

Address = 0x57h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	"Reserved for factory use only"							
Default	"Reserved for factory use only"							
Access	N/A							

Name	Description	Notes
N/A	Reserved for factory use	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

BUCK4 REGISTERS

B4_REG00 – Buck4 Configuration Register

Buck4 Address = 0x60h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	B4_PWR_GOOD	B4_OV	B4_ILIM	RFU	RFU	B4_ILIM_FLTMSK	B4_UV_FLTMSK	B4_OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
B4_PWR_GOOD	0 – Buck4 voltage is below the power good threshold 1 – Buck4 voltage is above the power good threshold	Provides real-time power good status
B4_OV	0 – Buck4 voltage is above the overvoltage threshold 1 – Buck4voltage is below the overvoltage threshold	Provides real-time overvoltage status
B4_ILIM	0 – Buck4 is below the ILIM threshold 1 – Buck4 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
B4_ILIM_FLTMSK	0 - Unmasks the Buck4 B4_ILIM register 1 - Masks the Buck4 B4_ILIM register	When 1, the B4_ILIM fault bit is masked from the master ILIM fault register, MSTR04. B4_ILIM still provides real-time current limit status.
B4_UV_FLTMSK	0 - Unmasks the Buck4 B4_UV register 1 - Masks the Buck4 B4_UV register	When 1, the B4_UV fault bit is masked from the master UV fault register, MSTR06. B4_UV still provides real-time current limit status.
B4_OV_FLTMSK	0 - Unmasks the Buck4 B4_OV register 1 - Masks the Buck4 B4_OV register	When 1, the B4_OV fault bit is masked from the master OV fault register, MSTR05. B4_OV still provides real-time overvoltage status.

B4_VSET00 – Buck4 Voltage Set0 Register

Buck4 Address = 0x61h	Default = 0xC8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B1_VSET0[7:0]							
Default	11001000							
Access	R/W							

Name	Description	Notes
B4_VSET0[7:0]	Buck4 output voltage setting in ACTIVE mode.	Controls the Buck4 output voltage. B4_VSET0 is used in ACTIVE mode. The output voltage is equal to B4_VSET * 0.0125 + 0.8V

B4_VSET01 – Buck4 Voltage Set1 Register

Address = 0x62h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B4_VSET1[7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
B4_VSET1[7:0]	Buck4 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck4 output voltage. B4_VSET1 is used in DVS or SLEEP modes. The output voltage is equal to B4_VSET1 * 0.0125 + 0.8V

B4_REG03 – Buck4 Configuration Register

Address = 0x63h	Default = 0xD4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_RAMP[2:0]		
Default	1	1	0	1	0	100		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON	0 – Buck4 is enabled through normal sequencing routing 1 – Buck4 I2C enable that bypasses normal sequencing	
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck4 shuts down when its sequenced input shuts down 1 – Buck4 stays on when its sequenced input shuts down	
SLEEPEN	0 – Buck4 stays on when the IC enters Sleep mode 1 – Buck4 turns off when the IC enters Sleep mode	
DREN	0 - Unmasks the Buck4 POK signal 1 - Masks the Buck4 POK signal	When 1, the Buck4 POK signal is masked and does not go to the master controller. This prevents Buck4 from asserting the nRESET pin when it is disabled or drops out of regulation.
SS_RAMP[2:0]	000 = 300us 001 = 400us 010 = 500us 011 = 600us 100 = 700us 101 = 800us 110 = 000us 111 = 1000us	Buck4 softstart ramp timing.

B4_REG04 – Buck4 Configuration Register

Address = 0x64h	Default = 0x81h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			001		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck4 does not affect nRESET_AUX1 output 1 – Buck4 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B4_REG05 – Buck4 Configuration Register

Address = 0x65h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
Default	0000				10		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SLEW[1:0]	00 = not allowed 01 = 14mV/us 10 = 3.5mV/us 11 = 0.88mV/us	Sets Buck4 slew rate when changing between VSET0 and VSET1 voltages. During the transition between voltages, PWR_GOOD, OV, and ILIM are automatically masked to avoid nRESET assertion. Setting to 00 is not allowed.
DBSTBY[1:0]	Determines sleep mode inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B4_REG06 – Buck4 Configuration Register

Address = 0x66h	Default = 0xCEh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	DISLPM	ONDLY[2:0]			DRVADJ[1:0]	
Default	1	1	0	011			00	
Access	R/W	R/W	R/W	R/W			R/W	

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	The PHASE bit aligns the converter switching to the rising or falling clock edge.
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	The PHASE_DELAY bit aligns the converter switching to the clock edge or to a 100ns delay from the clock edge.
DISLPM	0 – Low Power Mode enabled 1 – Low Power Mode disabled	
ONDLY[3:0]	000 34.5µs 001 106.5 µs 010 206.5 µs 011 306.5 µs 100 406.5 µs 101 506.5 µs 110 606.5 µs 111 706.5 µs	Programs the delay time between the Buck4 input trigger and when it turns on.
DRVADJ[1:0]	00 = 6.3ns rise time, 9.0ns fall time 01 = 4.5ns rise time, 7.4ns fall time 10 = 3.1ns rise time, 5.9ns fall time 11 = 3.0ns rise time, 5.0ns fall time	Sets the Buck4 switching rise and fall times. Faster rise time give higher efficiency while slower times give lower noise and EMI. These times change with Vin, load current, inductor value, etc and are intended to provide relative timing between settings.

B4_REG07 – Buck4 Configuration Register

Address = 0x67h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	"Reserved for factory use only"							
Default	"Reserved for factory use only"							
Access	N/A							

Name	Description	Notes
N/A	Reserved for factory use	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO1 REGISTERS

LDO1_REG00 – LDO1 Configuration Register

LDO1 Address = 0x70h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU[1:0]		ILIM_FLTMSK_LDO1	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1
Default	0	0	0	00		0	0	0
Access	RO	RO	RO	RO		R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD_LDO1	0 – LDO1 voltage is below the power good threshold 1 – LDO1 voltage is above the power good threshold	Provides real-time power good status
OV_LDO1	0 – LDO1 voltage is above the overvoltage threshold 1 – LDO1voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM_LDO1	0 – LDO1 is below the ILIM threshold 1 – LDO1 is above the ILIM threshold	Provides real-time current limit status
RFU[1:0]	Reserved for future use	Can write to this register, but it always returns a 0 when read.
ILIM_FLTMSK_LDO1	0 - Unmasks the LDO1 ILIM_LDO1 register 1 - Masks the LDO1 ILIM_LDO1 register	When 1, the ILIM_LDO1 fault bit is masked from the master ILIM fault register, MSTR04. ILIM_LDO1 still provides real-time current limit status.
UV_FLTMSK_LDO1	0 - Unmasks the LDO1 UV_LDO1 register 1 - Masks the LDO1 UV_LDO1 register	When 1, the UV_LDO1 fault bit is masked from the master UV fault register, MSTR06. UV_LDO1 still provides real-time current limit status.
OV_FLTMSK_LDO1	0 - Unmasks the LDO1 OV_LDO1 register 1 - Masks the LDO1 OV_LDO1 register	When 1, the OV_LDO1 fault bit is masked from the master OV fault register, MSTR05. OV_LDO1 still provides real-time overvoltage status.

LDO1_VSET – LDO1 Voltage Set0 Register

LDO1 Address = 0x71h	Default = 0x64h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	LDO1_VSET[6:0]						
Default	0	1100100						
Access	RO	R/W						

Name	Description	Notes
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
LDO1_VSET[7:0]	LDO1 output voltage setting.	Controls the LDO1 output voltage. The output voltage is equal to LDO1_VSET * 0.025 + 0.8V

LDO1_REG02 – LDO1 Configuration Register

Address = 0x72h	Default = 0xC3h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	RFU	SS_RAMP[1:0]	
Default	1	1	0	0	0	0	11	
Access	R/W	R/W	R/W	R/W	R/W	RO	R/W	

Name	Description			Notes
ON	0 – LDO1 is enabled through normal sequencing 1 – LDO1 is enabled via I2C that bypasses normal sequencing			
PBINEN	Determines startup sequencing from the CMI code			This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – LDO1 shuts down when its sequenced input shuts down 1 – LDO1 stays on when its sequenced input shuts down			
SLEEPEN	0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode			
DREN	0 - Unmasks the LDO1 POK signal 1 - Masks the LDO1 POK signal			When 1, the LDO1 POK signal is masked and does not go to the master controller. This prevents LDO1 from asserting the nRESET pin when it is disabled or drops out of regulation.
RFU	Reserved for future use			Can write to this register, but it always returns a 0 when read.
SS_RAMP[1:0]	Vout=1.8V	Vout=2.5V	Vout=3.3V	LDO1 softstart ramp timing. Note that the timing is variable depending on the output voltage setpoint.
	00 = 240us 01 = 330us 10 = 450us 11 = 575us	00 = not allowed 01 = 385us 10 = 465us 11 = 600us	00 = not allowed 01 = 450us 10 = 525us 11 = 660us	

LDO1_REG03 – LDO1 Configuration Register

Address = 0x73h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – LDO1 does not affect nRESET_AUX1 output 1 – LDO1 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO1_REG04 – LDO1 Configuration Register

Address = 0x74h	Default = 0x02h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ONDLY[2:0]			DIS_PULLDOWN
Default	0000				001			0
Access	R/W				R/W			R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ONDLY[2:0]	000 34.5µs 001 106.5 µs 010 206.5 µs 011 306.5 µs 100 406.5 µs 101 506.5 µs 110 606.5 µs 111 706.5 µs	Programs the delay time between the LDO1 input trigger and when it turns on.
DIS_PULLDOWN	0 – LDO1 discharge switch is enabled with LDO1 is turned off 1 – LDO1 discharge switch is always disabled	

LDO1_REG08 – LDO1 Configuration Register

Address = 0x78h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
RFU[7:0]	Reserved for factory use	Do not write to these bits in this register. Reading these bits returns random data.

LDO1_REG09 – LDO1 Configuration Register

Address = 0x79h	Default = 0xFFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B1_ILIM[1:0]		B2_ILIM[1:0]		B3_ILIM[1:0]		B4_ILIM[1:0]	
Default	11		11		11		11	
Access	R/W		R/W		R/W		R/W	

Name	Description	Notes
B1_ILIM[1:0]	00 = 5.3A 01 = 4.6A 10 = 3.8A 11 = 3.0A	Buck1 cycle-by-cycle peak current limit threshold.
B2_ILIM[1:0]	Same as B1_LIM	
B3_ILIM[1:0]	Same as B1_LIM	
B4_ILIM[1:0]	Same as B1_LIM	

LDO1_REG0A – LDO1 Configuration Register

Address = 0x7Ah	Default = 0x68h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO1_ILIM[1:0]		LDO2_ILIM[1:0]		LDO3_ILIM[1:0]		RFU[1:0]	
Default	01		10		10		00	
Access	R/W		R/W		R/W		R/W	

Name	Description	Notes
LDO1_ILIM[1:0]	00 = 350mA 01 = 500mA 10 = 630mA 11 = 1000mA	LDO1 output current limit.
LDO2_ILIM[1:0]	00 = 80mA 01 = 145mA 10 = 225mA 11 = 290mA	
LDO3_ILIM[1:0]	Same as LDO2_LIM	
N/A	Reserved for factory use	Can be used as a general purpose R/W scratch bit.

LDO1_REG0B – LDO1 Configuration Register

Address = 0x7Bh	Default = 0x8Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B4_LSASYNC	B3_LSASYNC	B2_LSASYNC	B1_LSASYNC	B4_LP_MODE	B3_LP_MODE	B2_LP_MODE	B1_LP_MODE
Default	1	0	0	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
B4_LSASYNC	0 - Normal synchronous operation 1 – Buck4 low side FET does not turn on when in Burst mode	
B3_LSASYNC	0 - Normal synchronous operation 1 – Buck3 low side FET does not turn on when in Burst mode	
B2_LSASYNC	0 - Normal synchronous operation 1 – Buck2 low side FET does not turn on when in Burst mode	
B1_LSASYNC	0 - Normal synchronous operation 1 – Buck1 low side FET does not turn on when in Burst mode	
B4_LP_MODE	0 – Normal Burst Mode operation 1 – Consumes less power in Burst Mode operation	When set to 0, the IC consumes more power in Burst Mode, but will have better performance transitioning from Burst Mode to normal operation.
B3_LP_MODE	0 – Normal Burst Mode operation 1 – Consumes less power in Burst Mode operation	
B2_LP_MODE	0 – Normal Burst Mode operation 1 – Consumes less power in Burst Mode operation	
B1_LP_MODE	0 – Normal Burst Mode operation 1 – Consumes less power in Burst Mode operation	

LDO1_REG0C – LDO1 Configuration Register

Address = 0x7Ch	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B4_HalfFreq	B3_HalfFreq	B2_HalfFreq	B1_HalfFreq	B4_DisPulldown	B3_DisPulldown	B2_DisPulldown	B1_DisPulldown
Default	0	0	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
B4_HalfFreq	0 – Sets Buck4 switch frequency to 2.25Mhz 1 - Sets Buck4 switch frequency to 1.125Mhz	Allows lower frequency operation to improve efficiency
B3_HalfFreq	0 – Sets Buck3 switch frequency to 2.25Mhz 1 - Sets Buck3 switch frequency to 1.125Mhz	Allows lower frequency operation to improve efficiency
B2_HalfFreq	0 – Sets Buck2 switch frequency to 2.25Mhz 1 - Sets Buck2 switch frequency to 1.125Mhz	Allows lower frequency operation to improve efficiency
B1_HalfFreq	0 – Sets Buck1 switch frequency to 2.25Mhz 1 - Sets Buck1 switch frequency to 1.125Mhz	Allows lower frequency operation to improve efficiency
B4_DisPulldown	0 - Enables the Buck4 output discharge FET. 1 - Disables the Buck4 output discharge FET.	
B3_DisPulldown	0 - Enables the Buck3 output discharge FET. 1 - Disables the Buck3 output discharge FET.	
B2_DisPulldown	0 - Enables the Buck2 output discharge FET. 1 - Disables the Buck2 output discharge FET.	
B1_DisPulldown	0 - Enables the Buck1 output discharge FET. 1 - Disables the Buck1 output discharge FET.	

DO23 REGISTERS

LDO23_REG00 – LDO2 Configuration Register

Address = 0x80h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO2	OV_LDO2	ILIM_LDO2	RFU[1:0]		ILIM_FLTMSK_LDO2	UV_FLTMSK_LDO2	OV_FLTMSK_LDO2
Default	0	0	0	0		0	0	0
Access	RO	RO	RO	R/W		R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD_LDO2	0 – LDO2 voltage is below the power good threshold 1 – LDO2 voltage is above the power good threshold	Provides real-time power good status
OV_LDO2	0 – LDO2 voltage is above the overvoltage threshold 1 – LDO2voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM_LDO2	0 – LDO2 is below the ILIM threshold 1 – LDO2 is above the ILIM threshold	Provides real-time current limit status
RFU[1:0]	Reserved for future use	Can be used as a general purpose R/W scratch bit.
ILIM_FLTMSK_LDO2	0 - Unmasks the LDO2 ILIM_LDO2 register 1 - Masks the LDO2 ILIM_LDO2 register	When 1, the LDO2_ILIM fault bit is masked from the master ILIM fault register, MSTR04. LDO2_ILIM still provides real-time current limit status.
UV_FLTMSK_LDO2	0 - Unmasks the LDO2 UV_LDO2 register 1 - Masks the LDO2 UV_LDO2 register	When 1, the LDO2_UV fault bit is masked from the master UV fault register, MSTR06. LDO2_UV still provides real-time current limit status.
OV_FLTMSK_LDO2	0 - Unmasks the LDO2 OV_LDO2 register 1 - Masks the LDO2 OV_LDO2 register	When 1, the OV_LDO2 fault bit is masked from the master OV fault register, MSTR05. OV_LDO2 still provides real-time overvoltage status.

LDO23_VSET – LDO2 Voltage Set0 Register

Address = 0x81h	Default = 0x28h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	LDO2_VSET[6:0]						
Default	0	0101000						
Access	RO	R/W						

Name	Description	Notes
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
LDO2_VSET[6:0]	LDO2 output voltage setting.	Controls the LDO2 output voltage. The output voltage is equal to LDO2_VSET * 0.025 + 0.8V

LDO23_REG02 – LDO2 Configuration Register

Address = 0x82h	Default = 0xC2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	RFU	SS_RAMP[1:0]	
Default	1	1	0	0	0	0	10	
Access	R/W	R/W	R/W	R/W	R/W	RO	R/W	

Name	Description			Notes
ON	0 – LDO2 is enabled through normal sequencing 1 – LDO2 is enabled via I2C that bypasses normal sequencing			
PBINEN	Determines startup sequencing from the CMI code			This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – LDO2 shuts down when its sequenced input shuts down 1 – LDO2 stays on when its sequenced input shuts down			
SLEEPEN	0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode			
DREN	0 - Unmasks the LDO2 POK signal 1 - Masks the LDO2 POK signal			When 1, the LDO2 POK signal is masked and does not go to the master controller. This prevents LDO2 from asserting the nRESET pin when it is disabled or drops out of regulation.
RFU	Reserved for future use			Can write to this register, but it always returns a 0 when read.
SS_RAMP[1:0]	Vout=1.8V	Vout=2.5V	Vout=3.3V	LDO2 softstart ramp timing.
	00 = 110us 01 = 110us 10 = 165us 11 = 215us	00 = 145us 01 = 145us 10 = 175us 11 = 215us	00 = 200us 01 = 200us 10 = 210us 11 = 235us	

LDO23_REG03 – LDO2 Configuration Register

Address = 0x83h	Default = 0x8Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	001			010		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – LDO2 does not affect nRESET_AUX1 output 1 – LDO2 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO23_REG04 – LDO2 Configuration Register

Address = 0x84h	Default = 0x06h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ONDLY[2:0]			DIS_PULLDOWN
Default	0000				011			0
Access	R/W				R/W			R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ONDLY[2:0]	000 34.5µs 001 106.5 µs 010 206.5 µs 011 306.5 µs 100 406.5 µs 101 506.5 µs 110 606.5 µs 111 706.5 µs	Programs the delay time between the LDO2 input trigger and when it turns on.
DIS_PULLDOWN	0 – LDO2 discharge switch is enabled with LDO2 is turned off 1 – LDO2 discharge switch is always disabled	

LDO23_REG08 – LDO3 Configuration Register

Address = 0x88h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO3	OV_LDO3	ILIM_LDO3	RFU[1:0]		ILIM_FLTMSK_LDO3	UV_FLTMSK_LDO3	OV_FLTMSK_LDO3
Default	0	0	0	0		0	0	0
Access	RO	RO	RO	RO		R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD_LDO3	0 – LDO3 voltage is below the power good threshold 1 – LDO3 voltage is above the power good threshold	Provides real-time power good status
OV_LDO3	0 – LDO3 voltage is above the overvoltage threshold 1 – LDO3voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM_LDO3	0 – LDO3 is below the ILIM threshold 1 – LDO3 is above the ILIM threshold	Provides real-time current limit status
RFU[1:0]	Reserved for future use	Can write to this register, but it always returns a 0 when read.
ILIM_FLTMSK_LDO3	0 - Unmasks the LDO3 ILIM_LDO3 register 1 - Masks the LDO3 ILIM_LDO3 register	When 1, the ILIM_LDO3 fault bit is masked from the master ILIM fault register, MSTR04. ILIM_LDO3 still provides real-time current limit status.
UV_FLTMSK_LDO3	0 - Unmasks the LDO3 UV_LDO3 register 1 - Masks the LDO3 UV_LDO3 register	When 1, the UV_LDO3 fault bit is masked from the master UV fault register, MSTR06. UV_LDO3 still provides real-time current limit status.
OV_FLTMSK_LDO3	0 - Unmasks the LDO3 OV_LDO3 register 1 - Masks the LDO3 OV_LDO3 register	When 1, the OV_LDO3 fault bit is masked from the master OV fault register, MSTR05. OV_LDO3 still provides real-time overvoltage status.

LDO23_VSET – LDO3 Voltage Set0 Register

Address = 0x89h	Default = 0x44h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	LDO3_VSET[6:0]						
Default	0	1000100						
Access	RO	R/W						

Name	Description	Notes
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
LDO3_VSET0[6:0]	LDO3 output voltage setting.	Controls the LDO3 output voltage. The output voltage is equal to LDO3_VSET * 0.025 + 0.8V

LDO23_REG0A – LDO3 Configuration Register

Address = 0x8Ah	Default = 0xC2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	RFU	SS_RAMP[1:0]	
Default	1	1	0	0	0	0	10	
Access	R/W	R/W	R/W	R/W	R/W	RO	R/W	

Name	Description			Notes
ON	0 – LDO3 is enabled through normal sequencing 1 – LDO3 is enabled via I2C that bypasses normal sequencing			
PBINEN	Determines startup sequencing from the CMI code			Do not change this bit
QLTCH	0 – LDO3 shuts down when its sequenced input shuts down 1 – LDO3 stays on when its sequenced input shuts down			
SLEEPEN	0 – LDO3 stays on when the IC enters Sleep mode 1 – LDO3 turns off when the IC enters Sleep mode			
DREN	0 - Unmasks the LDO3 POK signal 1 - Masks the LDO3 POK signal			This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RFU	Reserved for future use			Can write to this register, but it always returns a 0 when read.
SS_RAMP[1:0]	Vout=1.8V	Vout=2.5V	Vout=3.3V	LDO2 softstart ramp timing.
	00 = 110us 01 = 110us 10 = 165us 11 = 215us	00 = 145us 01 = 145us 10 = 175us 11 = 215us	00 = 200us 01 = 200us 10 = 210us 11 = 235us	

LDO23_REG0B – LDO3 Configuration Register

Address = 0x8Bh	Default = 0x93h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	010			011		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – LDO3 does not affect nRESET_AUX1 output 1 – LDO3 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO23_REG0C – LDO3 Configuration Register

Address = 0x8Ch	Default = 0x06h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ONDLY[2:0]			DIS_PULLDOWN
Default	0000				011			0
Access	R/W				R/W			R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ONDLY[2:0]	000 34.5µs 001 106.5 µs 010 206.5 µs 011 306.5 µs 100 406.5 µs 101 506.5 µs 110 606.5 µs 111 706.5 µs	Programs the delay time between the LDO3 input trigger and when it turns on.
DIS_PULLDOWN	0 – LDO3 discharge switch is enabled with LDO3 is turned off 1 – LDO3 discharge switch is always disabled	

References

1. *ACT8870 Datasheet*