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I²C Protocol for programming the ACT8945A

TABLE OF CONTENTS

1. INTRODUCTION

The ACT8945A is a complete, cost effective, highly efficient *ActivePMU™* power management solution, optimized for the unique power, voltage sequencing, and control requirements of the Atmel SAMA5D3 series: SAMA5D[31/33/34/35/36], and Atmel SAM9 series: SAM9G[15/25/35/45/46], SAM9X[25/35], SAM9M[10/11], SAM9N[11/12] processors. It is ideal for a wide range of high performance portable handheld applications such as human-machine interfaces, control panels, smart grid infrastructures, network gateways, M2M systems, 2D barcode scanners, barcode printers, machine vision equipment, as well as home and commercial building automations, POS terminals, medical devices and white goods. This device integrates the *ActivePath™* complete battery charging and management system with seven power supply channels.

The ACT8945A features an I²C interface that allows advanced programming capability to enhance overall system performance. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400kHz (“Fast-Mode” operation) and uses standard I²C commands. I²C write-byte commands are used to program the ACT8945A, and I²C read-byte commands are used to read the ACT8945A’s internal registers. The ACT8945A always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011011x].
SDA is a bi-directional data line and SCL is a clock input. The master device initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is locked-in on the rising edge of SCL. Each packet of data is followed by an “Acknowledge” (ACK) bit, used to confirm that the data was transmitted successfully.

This application note describes how the ACT8945A can be programmed via the I²C interface.

2. PROGRAMMING THE ACT8945A

2.1 ENABLE / DISABLE CONTROL

During normal operation, each regulator may be enabled or disabled via the I^2C interface by writing to that regulator's ON[ ] bit. The regulator accept rising or falling edge of ON[ ] bit as on/off signal. To enable the regulator, clear ON[ ] to 0 first then set to 1. To disable the regulator, set ON[ ] to 1 first then clear it to 0.

All regulators can be disabled by setting MSTROFF [ ] bit to 1.

Address of ON[ ] bit of each DC/DC and MSTROFF [ ] bit is show in Table 1.

Table 1
ON[ ] bit and MSTROFF[ ] bit address

Output	Address	Bit	Name
REG1	0x22	[7]	ON
REG2	0x32	[7]	ON
REG3	0x42	[7]	ON
REG4	0x51	[7]	ON
REG5	0x55	[7]	ON
REG6	0x61	[7]	ON
REG7	0x65	[7]	ON
SYS	0x01	[5]	MSTROFF

2.2 STEP-DOWN DC/DC OUTPUT VOLTAGE SETTING

By default, each DC/DC regulator powers up and regulates to its default output voltage. Output voltage is selectable by setting VSEL pin that when VSEL is low, output voltage is programmed by VSET1[ ] bits, and when VSEL is high, output voltage is programmed by VSET2[ ] bits. However, once the system is enabled, each regulator's output voltage may be independently programmed to a different value, typically in order to minimize the power consumption of the microprocessor during some operating modes. Program the output voltages via the I2C serial interface by writing to the regulator's VSET1[ ] register if VSEL is low or VSET2[ ] register if VSEL is high as shown in Table 3.

Address of VSET1[ ] and VSET2[ ] of each DC/DC is show in Table 2.

Table 2
DC/DC Output Voltage Setting Register Map

Output	Address	Bit	Name
REG1	0x20	[5:0]	VSET1
REG1	0x21	[5:0]	VSET2
REG2	0x30	[5:0]	VSET1
REG2	0x31	[5:0]	VSET2
REG3	0x40	[5:0]	VSET1
REG3	0x41	[5:0]	VSET2

Table 3
REGx/VSET[ ] Output Voltage Setting

REGx/VSET[2:0]	REGx/VSET[5:3]							
	000	001	010	011	100	101	110	111
000	0.600	0.800	1.000	1.200	1.600	2.000	2.400	3.200
001	0.625	0.825	1.025	1.250	1.650	2.050	2.500	3.300
010	0.650	0.850	1.050	1.300	1.700	2.100	2.600	3.400
011	0.675	0.875	1.075	1.350	1.750	2.150	2.700	3.500
100	0.700	0.900	1.100	1.400	1.800	2.200	2.800	3.600
101	0.725	0.925	1.125	1.450	1.850	2.250	2.900	3.700
110	0.750	0.950	1.150	1.500	1.900	2.300	3.000	3.800
111	0.775	0.975	1.175	1.550	1.950	2.350	3.100	3.900

2.3 LDO OUTPUT VOLTAGE SETTING

By default, each LDO powers up and regulates to its default output voltage. Once the system is enabled, each output voltage may be independently programmed to a different value by writing to the regulator's VSET[ ] register via the I^2C serial interface as shown in Table 3.
Address of VSET[ ] of each LDO is show in Table 4.

Table 4
LDO Output Voltage Setting Register Map

Output	Address	Bit	Name
REG4	0x50	[5:0]	VSET
REG5	0x54	[5:0]	VSET
REG6	0x60	[5:0]	VSET
REG7	0x64	[5:0]	VSET

2.4 PROGRAM SYSTEM VOLTAGE MONITOR

The ACT8945A features a programmable system voltage monitor, which monitors the voltage at VSYS and compares it to a programmable threshold voltage. The programmable voltage threshold is programmed by SYSLEV[3:0], as shown in Table 5. There is a 200mV rising hysteresis on SYSLEV[ ] threshold.

The nSYSSTAT[ ] bit reflects the output of an internal voltage comparator that monitors V_{VSYS} relative to the SYSLEV[ ] voltage threshold, the value of nSYSSTAT[ ] = 1 when V_{VSYS} is lower than the SYSLEV[ ] voltage threshold, and nSYSSTAT[ ] = 0 when V_{VSYS} is higher than the SYSLEV[ ] voltage threshold. Note that the SYSLEV[ ] voltage threshold is defined for falling voltages, and that the comparator produces about 200mV of hysteresis at VSYS. As a result, once V_{VSYS} falls below the SYSLEV threshold, its voltage must increase by more than about 200mV to clear that condition.

After the IC is powered up, the ACT8945A responds in one of two ways when the voltage at VSYS falls below the SYSLEV[ ] voltage threshold:

1) If nSYSMODE[ ] = 1 (default case), when system voltage level interrupt is unmasked (nSYSLEVMSK [ ]=1) and V_{VSYS} falls below the programmable threshold, the ACT8945A asserts nIRQ, providing a software “under-voltage alarm”. The response to this interrupt is controlled by the CPU, but will typically initiate a controlled shutdown sequence either or alert the user that the battery is low. In this case the interrupt is cleared when V_{VSYS} rises up again above the SYSLEV rising threshold and nSYSSTAT[ ] is read via I2C.

2) If nSYSMODE[ ] = 0, when V_{VSYS} falls below the programmable threshold the ACT8945A shuts down, immediately disabling all regulators. This option is useful for implementing a programmable “undervoltage lockout” function that forces the system off when the battery voltage falls below the SYSLEV threshold voltage. Since this option does not support a controlled shutdown sequence, it is generally used as a "fail-safe" to shut the system down when the battery voltage is too low.

Table 5:
SYSLEV Falling Threshold

SYSLEV[3:0]	SYSLEV Falling Threshold (Hysteresis = 200mV)
0000	2.3
0001	2.4
0010	2.5
0011	2.6
0100	2.7
0101	2.8
0110	2.9
0111	3.0
1000	3.1
1001	3.2
1010	3.3
1011	3.4
1100	3.5
1101	3.6
1110	3.7
1111	3.8

Table 6:
Voltage Monitor bit address

Output	Address	Bit	Name
SYS	0x00	[6]	nSYSMODE
SYS	0x00	[5]	nSYSLEMSK
SYS	0x00	[4]	nSYSSTAT
SYS	0x00	[3:0]	SYSLEV

2.5 REGULATORS TURN-ON DELAY

Each regulator features a programmable Turn-on Delay which help ensure a reliable qualification. This delay is programmed by DELAY[2:0], as shown in Table 7.

Table 7:
REGx/DELAY[ ] Turn-On Delay

DELAY[2:0]	Turn-on delay
000	0ms
001	2ms
010	4ms
011	8ms
100	16ms
101	32ms
110	64ms
111	128ms

Table 8:
DELAY bit address

Output	Address	Bit	Name
REG1	0x22	[4:2]	DELAY
REG2	0x32	[4:2]	DELAY
REG3	0x42	[4:2]	DELAY
REG4	0x51	[4:2]	DELAY
REG5	0x55	[4:2]	DELAY
REG6	0x61	[4:2]	DELAY
REG7	0x65	[4:2]	DELAY

2.6 POWER-OK AND OUTPUT FAULT INTERRUPT

Each regulator features a power-OK status bit that can be read by the system microprocessor via the I^2C interface. If an output voltage is lower than the power-OK threshold, typically 7% below the programmed regulation voltage, that regulator's OK [ ] bit will be 0. If a regulator's nFLTMSK[ ] bit is set to 1, the ACT8945A will interrupt the processor if that regulator's output voltage falls below the power -OK threshold. In this case, nIRQ will assert low and remain asserted until either the regulator is turned off or back in regulation, and the OK[ ] bit has been read via I^2C.

Address of OK[ ] bit and nFLTMSK[ ] bit of each regulator is shown in Table 9.

Table 9:
OK[ ] bit and nFLTMSK[ ] bit address

Output	Address	Bit	Name
REG1	0x22	[0]	OK
REG1	0x22	[1]	nFLTMSK
REG2	0x32	[0]	OK
REG2	0x32	[1]	nFLTMSK
REG3	0x42	[0]	OK
REG3	0x42	[1]	nFLTMSK
REG4	0x51	[0]	OK
REG4	0x51	[1]	nFLTMSK
REG5	0x55	[0]	OK
REG5	0x55	[1]	nFLTMSK
REG6	0x61	[0]	OK
REG6	0x61	[1]	nFLTMSK
REG7	0x65	[0]	OK
REG7	0x65	[1]	nFLTMSK

2.7 LDO OUTPUT DISCHARGE SETTING

Each of the ACT8945A's LDOs features an optional output discharge function, which discharges the output to ground through a 1.5kΩ resistance when the LDO is disabled. This feature may be enabled or disabled by setting DIS[ ]; set DIS[ ] to 1 to enable this function, clear DIS[ ] to 0 to disable it. Address of DIS[ ] bit of each LDO is shown in Table 10.

Table 10:
DIS bit address

Output	Address	Bit	Name
REG4	0x51	[6]	DIS
REG5	0x55	[6]	DIS
REG6	0x61	[6]	DIS
REG7	0x65	[6]	DIS

2.8 LDO LOW-POWER MODE SETTING

Each of ACT8945A's LDOs features a LOWIQ[ ] bit which, when set to 1, reduces the LDO's quiescent current by about 16%, saving power and extending battery lifetime. In low-power mode, Power Supply Rejection Ratio (PSRR) is reduced by about 10dB. Address of DIS[ ] bit of each LDO is shown in Table 11.

Table 11:
LOWIQ bit address

Output	Address	Bit	Name
REG4	0x51	[5]	LOWIQ
REG5	0x55	[5]	LOWIQ
REG6	0x61	[5]	LOWIQ
REG7	0x65	[5]	LOWIQ

2.9 *ActivePath*™ INPUT OVER-VOLTAGE PROTECTION

The *ActivePath*™ circuitry features input over-voltage protection circuitry. This circuitry disables charging when the input voltage exceeds the voltage set by OVPSET[ ] as shown in Table 12, but stands off the input voltage in order to protect the system. Note that the adjustable OVP threshold is intended to provide the charge cycle with adjustable immunity against upward voltage transients on the input, and is not intended to allow continuous charging with input voltages above the charger's normal operating voltage range. Independent of the OVPSET[ ] setting, the charge cycle is not allowed to resume until the input voltage falls back into the charger's normal operating voltage range (i.e. below 6.0V).

Table 12:
Input Over-Voltage Protection Setting

OVPSET[1:0]	OVP Setting Voltage
00	6.6V
01	7.0V
10	7.5V
11	8.0V

2.10 *ActivePath*™ CHARGER INTERRUPTS SETTING

2.10.1 Input Interrupts

An interrupt is generated any time the input supply is connected when INSTAT[ ] bit is set to 1 and the INCON[ ] bit is set to 1, and an interrupt is generated any time the input supply is disconnected when INSTAT[ ] bit is set to 1 and the NDIS[ ] bit is set to 1.

INDAT[ ] indicates the status of the CHGIN input supply. A value of 1 indicates hat a valid CHGIN input (CHGIN UVLO Threshold < VCHGIN < CHGIN OVP Threshold) is present, a value of 0 indicates a valid input is not present.

When an interrupt is generated by the input supply, reading the INSTAT[ ] returns a value of 1. INSTAT [ ] is automatically cleared to 0 upon reading. When no interrupt is generated by the input supply, reading the INSTAT[ ] returns a value of 0.

The state of the ACIN input can be read at any time by reading the ACINSTAT[ ] bit, where a value of 1 indicates that the voltage at ACIN is above the 1.2V threshold (indicating that a wall-cube has been attached), and a value of 0 indicates that the voltage is below this threshold.

2.10.2 State Machine Interrupts

The charger features the ability to generate interrupts when the charger state machine transitions, based upon the status of the CHG_ bits. Set CHGEOCIN[ ] bit to 1 and CHGSTAT[ ] bit to 1 to generate an interrupt when the charger state machine goes into the END-OF-CHARGE (EOC) state. Set CHGEOCOUT[ ] bit to 1 and CHGSTAT[ ] bit to 1 to generate an interrupt when the charger state machine exits the EOC state.
CHGDAT[ ] indicates the status of the charger state machine. A value of 1 indicates that the charger state machine is in END-OF-CHARGE state, a value of 0 indicates the charger state machine is in other states.

When an interrupt is generated by the charger state machine, reading the CHGSTAT[ ] returns a value of 1. CHGSTAT[ ] is automatically cleared to 0 upon reading. When no interrupt is generated by the charger state machine, reading the CHGSTAT[ ] returns a value of 0.

For additional information about the charge cycle, CSTATE[1:0] may be read at any time via I2C to determine the current charging state.

Table 13:
Charging Status Indication

CSTATE[1:0]	Charging Status
00	PRECONDITION State
01	FAST-CHARGE/ TOP-OFF State
10	END-OF-CHARGE State
11	SUSPEND/DISABLED/ FAULT State

2.10.3 Battery Temperature Interrupts

In order to ease detecting the status of the battery temperature, the charger features the ability to generate interrupts based upon the status of the battery temperature. Set the TEMPOUT[ ] bit to 1 and TEMPSTAT[ ] bit to 1 to generate an interrupt when battery temperature goes out of the valid temperature range. Set the TEMPIN[ ] bit to 1 and TEMPSTAT[ ] bit to 1 to generate an interrupt when battery temperature returns to the valid range.

TEMPDAT[ ] indicates the status of the battery temperature. A value of 1 indicates the battery temperature is inside of the valid range, a value of 0 indicates the battery is outside of the valid range.

When an interrupt is generated by the battery temperature event, reading the TEMPSTAT[ ] returns a value of 1. TEMPSTAT[ ] is automatically cleared to 0 upon reading. When no interrupt is generated by the battery temperature event, reading the TEMPSTAT[ ] returns a value of 0.

2.10.4 Charger Timer Interrupts

The charger features the ability to generate interrupts based upon the status of the charge timers. Set the TIMRPRE[ ] bit to 1 and TIMRSTAT[ ] bit to 1 to generate an interrupt when the Precondition Timer expires. Set the TIMRTOT [ ] bit to 1 and TIMRSTAT[ ] bit to 1 to generate an interrupt when the Total-Charge Timer expires.

TIMRDAT[ ] indicates the status of the charge timers. A value of 1 indicates a precondition timeout
or a total charge time-out occurs, a value of 0 indicates other cases.
When an interrupt is generated by the charge timers, reading the TIMRSTAT[ ] returns a value of 1. TIMRSTAT[ ] is automatically cleared to 0 upon reading. When no interrupt is generated by the charge timers, reading the TIMRSTAT[ ] returns a value of 0.

2.11 CHARGE SAFETY TIMERS

The charger features programmable charge safety timers which help ensure a safe charge by detecting potentially damaged cells. These timers are programmable via the PRETIMO[1:0] and TOTTIMO[1:0] bits, as shown in Table 14 and Table 15. Note that in order to account for reduced charge current resulting from DCCC operation in thermal regulation mode, the charge time-out periods are extended proportionally to the reduction in charge current. As a result, the actual safety period may exceed the nominal timer period.

Table 14:
PRECONDITION Safety Timer Setting

PRETIMO[1:0]	PRECONDITION TIME-OUT PERIOD
00	40 mins
01	60 mins
10	80 mins
11	Disabled

Table 15:
Total Safety Timer Setting

TOTTIMO[1:0]	TOTAL TIME-OUT PERIOD
00	3 hrs
01	4 hrs
10	5 hrs
11	Disabled

Table 16:
***ActivePath*™ CHARGER bit address**

Output	Address	Bit	Name
APCH	0x78	[7]	TIMRSTAT
APCH	0x78	[6]	TEMSTAT
APCH	0x78	[5]	INSTAT
APCH	0x78	[4]	CHGSTAT
APCH	0x78	[3]	TIMRDAT
APCH	0x78	[2]	TEMPDAT
APCH	0x78	[1]	INDAT
APCH	0x78	[0]	CHGDAT
APCH	0x79	[7]	TIMRTOT
APCH	0x79	[6]	TEMPIN
APCH	0x79	[5]	INCON
APCH	0x79	[4]	CHGEOCIN
APCH	0x79	[3]	TIMRPRE
APCH	0x79	[2]	TEMPOUT
APCH	0x79	[1]	INDIS
APCH	0x79	[0]	CHGEOCOUT
APCH	0x7A	[5:4]	CSTATE
APCH	0x7A	[1]	ACINSTAT