ACT4911 Register Definitions – CMI 301

Abstract

This paper identifies and explains the ACT4911 internal registers that help make this IC flexible and configurable for many applications. It provides a short description of each register, its individual bits, their function, and default values. This application note is specific to the Code Matrix Index, CMI 301.

Introduction

The ACT4911 is an ActivePMU eFuse and power loss protection IC from Active-Semi. Its wide input and output operating range allows it to operate with a wide range of FPGA's, peripherals, microcontrollers, and solid-state drive applications. The ACT4911 includes a step up boost converter to charge a bank of storage capacitors and a DC/DC step down converter to convert the stored energy to maintain the desired output voltage during input voltage brownout or power loss. Each regulator can be configured for a wide range of output voltages through the I2C interface. It also provide an on-board ADC converter to monitor the system's state of health. The ADC is configurable and readable via the I2C interface.

Although the ACT4911 is programmed at the factory with a default configuration, these settings can be changed through the I2C interface to provide customized configurations optimized for a specific processor and/or end application. IC configurability includes many options such as ADC high/low limits, fault thresholds and responses, status, and more. Active-Semi identifies these configurations with a Code Matrix Index, CMI. An IC's CMI is identified by the last three digits at the end of the orderable part number. Note that this application note is specific to the ACT4911's CMI 301. Refer to the appropriate application note for register information for other CMI versions.

The ACT4911 contains the following register types:

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

I2C REGISTER MAP

ADDR (HEX)	7	6	5	4	3	2	1	0
BASIC VOLATILE								
0	RFU	RFU	RFU	RFU	RFU	CURRENT_STATE [2:0]		
1	PVIN_OV	THERMAL_SHUTDOWN	THERMAL_PWRDWN	THERMAL_ALERT	VIN_FAULT	ENPIN_OV	eFUSE_nPG	eFUSE_VINLOSS
2	eFUSE_ILIM_ALERT	eFUSE_OC_SHUTDOWN	LDO_UV	ENPIN_UV	STR_UV	STR_OV	STR_PG	BKIN_UV
3	BUCK_ILIM_SHUTDOWN	BUCK_ILIM_ALERT	BUCK_nPG	BUCK_COMPFAIL	ADC_DRDY_IRQ	HCHK_NG	SPLMNT_MODE	BOOTCAPFAIL
4	RFU	RFU	ADC_OUTRNGE_CH5	ADC_OUTRNGE_CH4	ADC_OUTRNGE_CH3	ADC_OUTRNGE_CH2	ADC_OUTRNGE_CH1	ADC_OUTRNGE_CH0
5	ADC_DOUT [13:6]							
6	RFU	RFU	ADC_DOUT [5:0]					
7	ADC_DATA_READY	ADC_VREF_SEL	ADC_VREF_BYPASS	ADC_CLK_HALF	RFU	ADC_CH_READ [2:0]		
8	ADC_SWAP	EN_ADC	ADC_ONE_SHOT	ADC_CH_SCAN	EN_ADCBUF	ADC_CH_CONV [2:0]		
9	MSTR_OK	RFU	RFU	CMP_BSET_HI	RFU	RFU	PVIN_nUV	eFUSE_ISETLOW
A	RFU	RFU	RFU	RFU	RFU	EN_STR10mASINK	FORCE_HLTHCHK	FORCE_PWROFF
B	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

BASIC NON-VOLATILE								
C	ADC_UV_THRCH0 [7:0]							
D	ADC_UV_THRCH1 [7:0]							
E	ADC_UV_THRCH2 [7:0]							
F	ADC_UV_THRCH3 [7:0]							
10	ADC_UV_THRCH4 [7:0]							
11	ADC_UV_THRCH5 [7:0]							
12	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
13	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
14	ADC_OV_THRCH0 [7:0]							
15	ADC_OV_THRCH1 [7:0]							
16	ADC_OV_THRCH2 [7:0]							
17	ADC_OV_THRCH3 [7:0]							
18	ADC_OV_THRCH4 [7:0]							
19	RFU	RFU	RFU	RFU	RFU	PLI_FUNC_SEL [1:0]		nDIS_BST
1A	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
1B	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
1C	PVIN_OV_IRQ_MASK	THML_SD_IRQ_MASK	THML_PD_IRQ_MASK	THML_ALERT_IRQ_MASK	VIN_FAULT_IRQ_MASK	ENPIN_OV_IRQ_MASK	eF_nPG_IRQ_MASK	eF_VL_IRQ_MASK
1D	eF_ILIM_ALERT_IRQ_MASK	eF_OC_SD_IRQ_MASK	LDO_UV_IRQ_MASK	ENPIN_UV_IRQ_MASK	STR_UV_IRQ_MASK	STR_OV_IRQ_MASK	STR_PG_IRQ_MASK	BKIN_UV_IRQ_MASK
1E	BK_ILIM_SD_IRQ_MASK	BK_ILIM_ALERT_IRQ_MASK	BK_nPG_IRQ_MASK	BK_COMPFAIL_IRQ_MASK	ADC_DRDY_IRQ_MASK	HCHK_NG_IRQ_MASK	SPLMNT_IRQ_MASK	BOOTCAPFAIL_IRQ_MASK
1F	ADC_OUTRNG_IRQ_MASK	GLOBAL_IRQ_MASK	DIS_HEALTH_CHK	RFU	HMON_TSET [3:0]			
20	EN_OV_REF [2:0]			EN_STARTDELAY	HMON_THR [3:0]			
21	EN_LATCH_SPLMNT	BST_CLIM [1:0]		BST_VSET [4:0]				
22	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

23	ADC_OS [7:0]							
24	ADC_GE [7:0]							
26	RFU	RFU	RFU	RFU	BK_DRVADJ[1:0]		BK_CLIM[1:0]	
27	RFU				SCALE_TSET_2X	SCALE_TSET_4X	SCALE_HCHK_2X	SCALE_HCHK_2X
28	RFU	BK_FREQ[2:0]			RFU[3:0]			
38	Mask_BKIN_nUV	Mask_eF_OC	Mask_eF_VIN_LT_VO	Mask_LDO_FAULT	Mask_STR_OV	Mask_STR_UV	Mask_BK_OV	Mask_BK_UV
3B	DEVICE ID[7:0]							

STATUS0 – Status Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[4:0]					CURRENT_STATE[2:0]		
Default	00000					000		
Access	RO					RO		

Name	Description	Notes
RFU[4:0]	Reserved for future use	Can write to this register, but it always returns a 0 when read.
CURRENT_STATE[2:0]	000 = UV/POR 001 = SOFTSTART 010 = NORMAL 011 = HEALTH CHECK 100 = SUPPLEMENT 101 = SHUTDOWN1 110 = SHUTDOWN2 111 = NA	Shows the current state of the state machine.

STATUS1 - Status Register

Address = 0x01h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PVIN_OV	THERMAL_ SHUTDOWN	THERMAL_ PWRDWN	THERMAL_ ALERT	VIN_FAULT	ENPIN_ OV	eFUSE_ nPG	eFUSE_VI NLOSS
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
PVIN_OV	0 = VIN < OVLO 1 = VIN > OVLO	When this bit = 1, nIRQ goes low if this function is not masked.
THERMAL_SHUTDOWN	0 = Junction temperature < 155 deg C. 1 = Junction temperature > 155 deg C.	Asserts nIRQ when =1 and the function is not masked.
THERMAL_PWRDWN	0 = Junction temperature < 145 deg C. 1 = Junction temperature < 145 deg C.	Asserts nIRQ when =1 and the function is not masked.
THERMAL_ALERT	0 = Junction temperature < 125 deg C. 1 = Junction temperature > 125 deg C.	Asserts nIRQ when =1 and the function is not masked.
VIN_FAULT	0 = no fault condition 1 = fault condition exists	VIN_FAULT is the logical OR of EN_UV, EN_OV, and PVIN_OV. Asserts nIRQ when =1 and the function is not masked.
ENPIN_OV	0 = EN is < OV_REF 1 = EN is > OV_REF	Used to check for VIN OV. Asserts nIRQ when =1 and the function is not masked.
eFUSE_nPG	0 = VIN - VOUT < 200mV 1 = VIN - VOUT > 560mV	When this bit = 1 (drop in output voltage), nIRQ goes low if this function is not masked.
eFUSE_VINLOSS	0 = VOUT - VIN < -390mV 1 = VOUT - VIN > 120mV	When this bit = 1 (drop in input voltage), nIRQ goes low if this function is not masked.

STATUS2 - Status Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	eFUSE_ILIM_ALERT	eFUSE_OC_SHUTDOWN	LDO_UV	ENPIN_UV	STR_UV	STR_OV	STR_PG	BKIN_UV
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
eFUSE_ILIM_ALERT	0 = ISET < 0.88V 1 = ISET > 0.9V	Asserts nIRQ when =1 and the function is not masked.
eFUSE_OC_SHUTDOWN	0 = eFuse current is below shutdown level 1 = eFuse current is above shutdown level	Asserts nIRQ when =1 and the function is not masked.
LDO_UV	0 = REF voltage is ready 1 = REF voltage is not ready	Asserts nIRQ when =1 and the function is not masked.
ENPIN_UV	0 = EN > 0.64V 1 = EN < 0.64V	Asserts nIRQ when = 1 and the function is not masked.
STR_UV	0 = STR voltage is > programmed under voltage limit 1 = STR voltage is < programmed under voltage limit	Asserts nIRQ when =1 and the function is not masked.
STR_OV	0 = STR voltage is < programmed over voltage limit 1 = STR voltage is > programmed over voltage limit	Asserts nIRQ when =1 and the function is not masked.
STR_PG	0 = STR voltage is < 90% of the setpoint 1 = STR voltage is target voltage	Asserts nIRQ when =1 and the function is not masked.
BKIN_UV	0 = STR > 4.0V 1 = STR < 3.6V at supplement state	When this bit = 1 (drop in input voltage), goes to UV/POR state

STATUS3 - Status Register

Address = 0x03h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	BUCK_ILIM_SHUTDOWN	BUCK_ILIM_ALERT	BUCK_nPG	BUCK_COMPFAIL	ADC_DRDY_IRQ	HCHK_NG	SPLMNT_MODE	BOOTCAPFAIL
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
BUCK_ILIM_SHUTDOWN	0 = Buck is below the ILIM2 threshold 1 = Buck is above the ILIM2 threshold	When this bit = 1, goes to UV/POR state
BUCK_ILIM_ALERT	0 = Buck is below the ILIM1 threshold 1 = Buck is above the ILIM1 threshold	Asserts nIRQ when =1 and the function is not masked.
BUCK_nPG	0 = Buck output is above the UV threshold 1 = Buck output is below the UV threshold	When this bit = 1, goes to UV/POR state
BUCK_COMPFAIL	0 = External impedance on COMP pin is ok 1 = COMP pin is shorted	Asserts nIRQ when =1 and the function is not masked.
ADC_DRDY_IRQ	0 = ADC has not finished conversion 1 = ADC has finished one shot conversion	Asserts nIRQ when =1. This bit is latched until read.
HCHK_NG	0 = No error at Health check 1 = Error at Health check	Asserts nIRQ when =1 and the function is not masked.
SPLMNT_MODE	0 = IC not in supplement mode 1 = IC is in supplement mode	Asserts nIRQ when =1. This bit is latched until read.
BOOTCAPFAIL	0 = HSB voltage is ready for switching 1 = HSB voltage is not ready for switching	Asserts nIRQ when =1 and the function is not masked.

ADC_RANGE – ADC Out of Range Register

Address = 0x04h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	ADC_OUTRNGE_CH7	ADC_OUTRNGE_CH7	ADC_OUTRNGE_CH7	ADC_OUTRNGE_CH7	ADC_OUTRNGE_CH7	ADC_OUTRNGE_CH7
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for future	This bit always returns a 0
RFU	Reserved for future	This bit always returns a 0
ADC_OUTRNGE_CH5	0 = ADC channel 5 is within range 1 = ADC channel 5 is out of range	Asserts nIRQ when =1. This bit is latched until read.
ADC_OUTRNGE_CH4	0 = ADC channel 4 is within range 1 = ADC channel 4 is out of range	Asserts nIRQ when =1. This bit is latched until read.
ADC_OUTRNGE_CH3	0 = ADC channel 3 is within range 1 = ADC channel 3 is out of range	Asserts nIRQ when =1. This bit is latched until read.
ADC_OUTRNGE_CH2	0 = ADC channel 2 is within range 1 = ADC channel 2 is out of range	Asserts nIRQ when =1. This bit is latched until read.
ADC_OUTRNGE_CH1	0 = ADC channel 1 is within range 1 = ADC channel 1 is out of range	Asserts nIRQ when =1. This bit is latched until read.
ADC_OUTRNGE_CH0	0 = ADC channel 0 is within range 1 = ADC channel 0 is out of range	Asserts nIRQ when =1. This bit is latched until read.

ADC1 – ADC Read Register

Address = 0x05h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_DOUT[13:6]							
Default	0x00h							
Access	RO							

Name	Description	Notes
ADC_DOUT[13:6]	Contains the most significant eight bits for the result of an ADC read. The ADC channel read is set by ADC_CH_READ[2:0]. The following equations calculate the measured value. CH0: Input Current (A) = (ADC_DOUT–128)*1.221/RLIM where RLIM is in kohm CH1: VIN Voltage (V) = (ADC_DOUT-128)*0.392 CH2: STR Voltage (V) = (ADC_DOUT-128)*0.392 CH3: VOUT Voltage (V) = (ADC_DOUT-128)*0.392 CH4: Die Temperature (deg C) = (ADC_DOUT*6.125)-1053.75	The register contains an 8 bit unsigned binary integer.

ADC2 – ADC Read Register

Address = 0x06h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[1:0]		ADC_DOUT[5:0]					
Default	00		000000					
Access	RO		RO					

Name	Description	Notes
RFU[1:0]	Reserved for future use	Always returns 00
ADC_DOUT[5:0]	Contains the least significant six bits for the result of an ADC read. See register 0x05h for details.	The register contains a dix bit unsigned binary integer.

ADC3 – ADC Configuration Register

Address = 0x07h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_DATA_READY	ADC_VREF_SEL	ADC_VREF_BYPASS	ADC_CLK_HALF	RFU	ADC_CH_READ[2:0]		
Default	0	0	0	0	0	0		
Access	RO	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ADC_DATA_READY	0 = ADC data is not ready to read 1 = ADC conversion is finished. Data is ready to read	Automatically cleared when ADC data is read from register 0x05h and 0x06h
ADC_VREF_SEL	N/A	Do not change this register value. Changing this value will result in unexpected IC behavior.
ADC_VREF_BYPASS	N/A	Do not change this register value. Changing this value will result in unexpected IC behavior.
ADC_CLK_HALF	0 = ADC operates at normal frequency 1 = ADC operates at half frequency	
RFU	Reserved for future use	Always returns 0
ADC_CH_READ[2:0]	000 = reads input current 001 = reads VIN voltage 010 = reads STR voltage 011 = reads VOUT voltage 100 = reads die temperature 101 = reads AGND voltage 110 = reads AGND voltage 111 = reads AGND voltage	Selects the desired ADC output to be read. Connects the ADC output to register ADC1 0x05h and 0x06h.

ADC4 – ADC Configuration Register

Address = 0x08h	Default = 0x10h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_SWAP	EN_ADC	ADC_ONE_SHOT	ADC_CH_SCAN	EN_ADCBUF	ADC_CH_CONV[2:0]		
Default	0	0	0	1	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ADC_SWAP	0 = ADC inputs have normal polarity 1 = Swaps ADC positive and negative inputs	Customer can read with both polarities and average the results to “zero out” the ADC input offsets.
EN_ADC	0 = ADC disabled 1 = ADC enabled	In one-time conversion mode, EN_ADC resets to 0 after each ADC conversion. Changing back to 1 initiates another ADC conversion.
ADC_ONE_SHOT	0 = ADC continually converts data when EN_ADC=1 1 = ADC performs a one-time conversion when EN_ADC=1	
ADC_CH_SCAN	0 = Scan single channel specified by ADC_CH_CONV 1 = Scan all channels	
EN_ADCBUF	0 = Disable ADC buffer 1 = Enable ADC buffer	
ADC_CH_CONV[2:0]	000 = Connects ADC input to the Input Current channel 001 = Connects ADC input to VIN channel 010 = Connects ADC input to STR channel 011 = Connects ADC input to the VOUT channel 100 = Connects ADC input to the temperature sensor 101 = Connects ADC input to the AGND channel 110 = Connects ADC input to the AGND channel 111 = Connects ADC input to the AGND channel	In ADC one shot mode (ADC_ONE_SHOT = 1) this register connects the ADC input to the input signal to be converted. Note that setting to 101, 110, 111 connects the ADC input to AGND signal.

STATUS4 - Status Register

Address = 0x09h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	MSTR_OK	RFU	RFU	CMP_BSET_HI	RFU[1:0]		PVIN_nUV	eFUSE_ISETLOW
Default	0	0	0	0	0		0	0
Access	RO	RO	RO	RO	RO		RO	RO

Name	Description	Notes
MSTR_OK	0 = Internal references are not ready 1 = Internal references are ready	
RFU	Reserved for future	Always returns a 0
RFU	Reserved for future	Always returns a 0 Always returns a 0
CMP_BSET_HI	0 = BSET < 1.5V 1 = BSET > 1.5V	This bit must always be equal to 0. Setting to 1 may result in unexpected IC behavior.
RFU[1:0]	Reserved for future use	Always returns a 00
PVIN_nUV	0 = VIN is above UVLO threshold 1 = VIN is below UVLO threshold	
eFUSE_ISETLOW	0 = ISET voltage is > 0.1V 1 = ISET voltage is < 0.08V	When = 1, indicates a short circuit on ISET

CONTROL1 - Control Register

Address = 0x0Ah	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[4:0]					EN_STR10mASINK	FORCE_HLTHCHK	FORCE_PWROFF
Default	00000					0	0	0
Access	RO					R/W	R/W	R/W

Name	Description	Notes
RFU[4:0]	Reserved for future use	Always returns 00010
EN_STR10mASINK	0 = Standard health check functionality 1 = Manually turns on the 10mA storage cap discharge current	When enabled, the IC sinks 10mA until the function is disabled.
FORCE_HLTHCHK	0 = Normal operation 1 = Forces a one-shot health check cycle	Forces a single health check event even if EN_HCHK=0. This bit automatically resets to 0 after the health check is completed.
FORCE_PWROFF	0 = Normal operation 1 = Forces IC into the UV/POR state	

RFU Register

Address = 0x0Bh	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
N/A	Reserved for factory use	Do not write to this register. Reading this register returns 0x00h

ADC_UV0 – ADC Undervoltage Threshold Register

Address = 0x0Ch	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_UV_THRCH0[7:0]							
Default	0x00h							
Access	R/W							

Name	Description	Notes
ADC_UV_THRCH0[7:0]	Lower threshold for ADC CH0	Asserts nIRQ when ADC CH 0 reads below this value.

ADC_UV1 – ADC Undervoltage Threshold Register

Address = 0x0Dh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_UV_THRCH1[7:0]							
Default	0x00h							
Access	R/W							

Name	Description	Notes
ADC_UV_THRCH1[7:0]	Lower threshold for ADC CH1	Asserts nIRQ when ADC CH1 reads below this value.

ADC_UV2 – ADC Undervoltage Threshold Register

Address = 0x0Eh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_UV_THRCH2[7:0]							
Default	0x00h							
Access	R/W							

Name	Description	Notes
ADC_UV_THRCH2[7:0]	Lower threshold for ADC CH2	Asserts nIRQ when ADC CH2 reads below this value.

ADC_UV3 – ADC Undervoltage Threshold Register

Address = 0x0Fh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_UV_THRCH3[7:0]							
Default	0x00h							
Access	R/W							

Name	Description	Notes
ADC_UV_THRCH3[7:0]	Lower threshold for ADC CH3	Asserts nIRQ when ADC CH3 reads below this value.

ADC_UV4 – ADC Undervoltage Threshold Register

Address = 0x10h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_UV_THRCH4[7:0]							
Default	0x00h							
Access	R/W							

Name	Description	Notes
ADC_UV_THRCH4[7:0]	Lower threshold for ADC CH4	Asserts nIRQ when ADC CH4 reads below this value.

ADC_UV5 – ADC Undervoltage Threshold Register

Address = 0x011h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_UV_THRCH5[7:0]							
Default	0x00h							
Access	R/W							

Name	Description	Notes
ADC_UV_THRCH5[7:0]	Lower threshold for ADC CH5	Asserts nIRQ when ADC CH5 reads below this value.

RFU Register

Address = 0x12h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	Reserved for factory use							
Default	Reserved for factory use							
Access	R/W							

Name	Description	Notes
N/A	Reserved for factory use	Do not write to this register. Reading this register returns 0x00h

RFU Register

Address = 0x13h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	Reserved for factory use							
Default	Reserved for factory use							
Access	R/W							

Name	Description	Notes
N/A	Reserved for factory use	Do not write to this register. Reading this register returns 0x00h

ADC_OV0 – ADC Overvoltage Threshold Register

Address = 0x14h	Default = 0xFFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_OV_THRCH0[7:0]							
Default	0xFFh							
Access	R/W							

Name	Description	Notes
ADC_OV_THRCH0[7:0]	Upper threshold for ADC CH0	Asserts nIRQ when ADC CH 0 reads above this value.

ADC_OV1 – ADC Overvoltage Threshold Register

Address = 0x15h	Default = 0xFFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_OV_THRCH1[7:0]							
Default	0xFFh							
Access	R/W							

Name	Description	Notes
ADC_OV_THRCH1[7:0]	Upper threshold for ADC CH1	Asserts nIRQ when ADC CH1 reads above this value.

ADC_OV2 – ADC Overvoltage Threshold Register

Address = 0x16h	Default = 0xFFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_OV_THRCH2[7:0]							
Default	0xFFh							
Access	R/W							

Name	Description	Notes
ADC_OV_THRCH2[7:0]	Upper threshold for ADC CH2	Asserts nIRQ when ADC CH2 reads above this value.

ADC_OV3 – ADC Overvoltage Threshold Register

Address = 0x17h	Default = 0xFFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_OV_THRCH3[7:0]							
Default	0xFFh							
Access	R/W							

Name	Description	Notes
ADC_OV_THRCH3[7:0]	Upper threshold for ADC CH3	Asserts nIRQ when ADC CH3 reads above this value.

ADC_OV4 – ADC Overvoltage Threshold Register

Address = 0x18h	Default = 0xFFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_OV_THRCH4[7:0]							
Default	0xFFh							
Access	R/W							

Name	Description	Notes
ADC_OV_THRCH4[7:0]	Upper threshold for ADC CH4	Asserts nIRQ when ADC CH4 reads above this value.

ADC_OV5 – PLI Configuration

Address = 0x19h	Default = 0xFFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[4:0]					PLI_FUNC_SEL[1:0]		nDIS_BST
Default	11111					11		11
Access	R/W							

Name	Description	Notes
RFU[4:0]	Reserved for future use	Always returns 11111. Do not change these values. Changing these values may result in unexpected IC behavior.
PLI_FUNC_SEL[1:0]	00 = PLI function enabled 01 = PG_STR function enabled 10 = VOUT_READY function enabled 11 = PLI & VOUT_READY function enabled	
nDIS_BST	0 = Boost is disabled 1 = Boost is enabled by state machine	

RFU Register

Address = 0x1Ah	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	Reserved for factory use							
Default	Reserved for factory use							
Access	R/W							

Name	Description	Notes
N/A	Reserved for factory use	Do not write to this register. Reading this register returns 0xFFh

RFU Register

Address = 0x1Bh	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	Reserved for factory use							
Default	Reserved for factory use							
Access	R/W							

Name	Description	Notes
N/A	Reserved for factory use	Do not write to this register. Reading this register returns 0xFFh

MASK1 – Masking Register

Address = 0x1Ch	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PVIN_OV_IRQ_MASK	THML_SD_IRQ_MASK	THML_PD_IRQ_MASK	THML_ALERT_IRQ_MASK	VIN_FAULT_IRQ_MASK	ENPIN_OV_IRQ_MASK	eF_nPG_IRQ_MASK	eF_VL_IRQ_MASK
Default	0	0	0	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PVIN_OV_IRQ_MASK	0 – unmasks the PVIN_OV register 1 – masks the PVIN_OV register	When 1, PVIN_OV register will not assert nIRQ. PVIN_OV register still provides a real-time status
THML_SD_IRQ_MASK	0 – unmasks the THERMAL_SHUTDOWN register 1 – masks the THERMAL_SHUTDOWN register	When 1, THERMAL_SHUTDOWN register will not assert nIRQ. THERMAL_SHUTDOWN register still provides a real-time status
THML_PD_IRQ_MASK	0 – unmasks the THERMAL_PWRDOWN register 1 – masks the THERMAL_PWRDOWN register	When 1, THERMAL_PWRDOWN register will not assert nIRQ. THERMAL_PWRDOWN register still provides a real-time status
THML_ALERT_IRQ_MASK	0 – unmasks the THERMAL_ALERT register 1 – masks the THERMAL_ALERT register	When 1, THERMAL_ALERT register will not assert nIRQ. THERMAL_ALERT register still provides a real-time status
VIN_FAULT_IRQ_MASK	0 – unmasks the VIN_FAULT register 1 – masks the VIN_FAULT register	When 1, VIN_FAULT register will not assert nIRQ. VIN_FAULT register still provides a real-time status
ENPIN_OV_IRQ_MASK	0 – unmasks the ENPIN_OV register 1 – masks the ENPIN_OV register	When 1, ENPIN_OV register will not assert nIRQ. ENPIN_OV register still provides a real-time status
eF_nPG_IRQ_MASK	0 – unmasks the eFUSE_nPG register 1 – masks the eFUSE_nPG register	When 1, eFUSE_nPG register will not assert nIRQ. eFUSE_nPG register still provides a real-time status
eF_VL_IRQ_MASK	0 – unmasks the eFUSE_VINLOSS register 1 – masks the eFUSE_VINLOSS register	When 1, eFUSE_VINLOSS register will not assert nIRQ. eFUSE_VINLOSS register still provides a real-time status

MASK2 – Masking Register

Address = 0x1Dh	Default = 0x12h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	eF_ILIM_ALERT_IRQ_MASK	eF_OC_SD_IRQ_MASK	LDO_UV_IRQ_MASK	ENPIN_UV_IRQ_MASK	STR_UV_IRQ_MASK	STR_OV_IRQ_MASK	STR_PG_IRQ_MASK	VHS_UV_IRQ_MASK
Default	0	0	0	1	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
eF_ILIM_ALERT_IRQ_MASK	0 – unmasks the eFUSE_ILIM_ALERT register 1 – masks the eFUSE_ILIM_ALERT register	When 1, eFUSE_ILIM_ALERT register will not assert nIRQ. eFUSE_ILIM_ALERT register still provides a real-time status
eF_OC_SD_IRQ_MASK	0 – unmasks the eFUSE_OC_SHUTDOWN register 1 – masks the eFUSE_OC_SHUTDOWN register	When 1, eFUSE_OC_SHUTDOWN register will not assert nIRQ. eFUSE_OC_SHUTDOWN register still provides a real-time status
LDO_UV_IRQ_MASK	0 – unmasks the LDO_UV register 1 – masks the LDO_UV register	When 1, LDO_UV register will not assert nIRQ. LDO_UV register still provides a real-time status
ENPIN_UV_IRQ_MASK	0 – unmasks the ENPVIN_UV register 1 – masks the ENPVIN_UV register	When 1, ENPVIN_UV register will not assert nIRQ. ENPVIN_UV register still provides a real-time status
STR_UV_IRQ_MASK	0 – unmasks the STR_UV register 1 – masks the STR_UV register	When 1, STR_UV register will not assert nIRQ. STR_UV register still provides a real-time status
STR_OV_IRQ_MASK	0 – unmasks the STR_OV register 1 – masks the STR_OV register	When 1, STR_OV register will not assert nIRQ. STR_OV register still provides a real-time status
STR_PG_IRQ_MASK	0 – unmasks the STR_PG register 1 – masks the STR_PG register	When 1, STR_PG register will not assert nIRQ. STR_PG register still provides a real-time status
BKIN_UV_IRQ_MASK	0 – unmasks the BKIN_UV register 1 – masks the BKIN_UV register	When 1, BKIN_UV register will not assert nIRQ. BKIN_UV register still provides a real-time status

MASK3 – Masking Register

Address = 0x1Eh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BK_ILIM_SD_IRQ_MASK	BK_ILIM_ALERT_IRQ_MASK	BK_nPG_IRQ_MASK	BK_COMPFAIL_IRQ_MASK	ADC_DRDY_IRQ_MASK	HCHK_NG_IRQ_MASK	SPLMNT_IRQ_MASK	BOOTCAPFAIL_IRQ_MASK
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
BK_ILIM_SD_IRQ_MASK	0 – unmasks the BUCK_ILIM_SHUTDOWN register 1 – masks the BUCK_ILIM_SHUTDOWN register	When 1, BUCK_ILIM_SHUTDOWN register will not assert nIRQ. BUCK_ILIM_SHUTDOWN register still provides a real-time status
BK_ILIM_ALERT_IRQ_MASK	0 – unmasks the BUCK_ILIM_ALERT register 1 – masks the BUCK_ILIM_ALERT register	When 1, BUCK_ILIM_ALERT register will not assert nIRQ. BUCK_ILIM_ALERT register still provides a real-time status
BK_nPG_IRQ_MASK	0 – unmasks the BUCK_nPG register 1 – masks the BUCK_nPG register	When 1, BUCK_nPG register will not assert nIRQ. BUCK_nPG register still provides a real-time status
BK_COMPFAIL_IRQ_MASK	0 – unmasks the BUCK_ COMPFAIL register 1 – masks the BUCK_ COMPFAIL register	When 1, BUCK_ COMPFAIL register will not assert nIRQ. BUCK_ COMPFAIL register still provides a real-time status
ADC_DRDY_IRQ_MASK	0 – unmasks the ADC_DRDY_IRQ register 1 – masks the ADC_DRDY_IRQ register	When 1, ADC_DRDY_IRQ register will not assert nIRQ. ADC_DRDY_IRQ register still provides a real-time status
HCHK_NG_IRQ_MASK	0 – unmasks the HCHK_NG register 1 – masks the HCHK_NG register	When 1, HCHK_NG register will not assert nIRQ. HCHK_NG register still provides a real-time status
SPLMNT_IRQ_MASK	0 – unmasks the SPLMNT_MODE register 1 – masks the SPLMNT_MODE register	When 1, SPLMNT_MODE register will not assert nIRQ. SPLMNT_MODE register still provides a real-time status
BOOTCAPFAIL_IRQ_MASK	0 – unmasks the BOOTCAPFAIL register 1 – masks the BOOTCAPFAIL register	When 1, BOOTCAPFAIL register will not assert nIRQ. BOOTCAPFAIL register still provides a real-time status

MASK4 – Masking Register

Address = 0x1Fh	Default = 0x04h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_OUTRNG_IRQ_MASK	GLOBAL_IRQ_MASK	DIS_HEALTH_CHK	RFU	HMON_TSET[3:0]			
Default	0	0	0	0	0100			
Access	R/W	R/W	R/W	RO	R/W			

Name	Description	Notes
ADC_OUTRNG_IRQ_MASK	0 – unmasks all ADC_OUTRNGE_CHx registers 1 – masks all ADC_OUTRNGE_CHx registers	When 1, ADC_OUTRNGE_CHx registers will not assert nIRQ. ADC_OUTRNGE_CHx registers still provide a real-time status
GLOBAL_IRQ_MASK	0 – unmasks inputs to the nIRQ pin 1 – masks inputs to the nIRQ pin	When 1, nIRQ is forced to be deasserted, regardless of any operating condition.
DIS_HEALTH_CHK	0 – Health check is enabled 1 – Health check is disabled	When disabled, Health Check can still be run by writing 1 into FORCE_HCHK
RFU	Reserved for future use	Can be used as a scratch bit.
HMON_TSET[3:0]	0000 = 2ms 0001 = 4ms 0010 = 8ms 0011 = 16ms 0100 = 32ms 0101 = 64ms 0110 = 128ms 0111 = 256ms 1000 = 384ms 1001 = 512ms 1010 = 640ms 1011 = 768ms 1100 = 896ms 1101 = 1024ms 1110 = 1152ms 1111 = 1280ms	Sets the Health Check current discharge time.

CONTROL3 - Control Register

Address = 0x20h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_OV_REF[2:0]			EN_STARTDELAY	HMON_THR[3:0]			
Default	010			0	0000			
Access	R/W			R/W	R/W			

Name	Description	Notes
EN_OV_REF[2:0]	000 = Disable 001 = 0.82V 010 = 0.92V 011 = 1.00V 100 = 1.08V 101 = 1.16V 110 = 1.24V 111 = 1.32V	EN_OV reference voltage.
EN_STARTDELAY	0 = Sets eFuse delay to 0ms 1 = Sets eFuse delay to 125ms	Delay time from VIN going above UV threshold to when the eFuse starts turning on
HMON_THR[3:0]	0000 = 95.0% 0001 = 95.2% 0010 = 95.4% 0011 = 95.6% 0100 = 95.8% 0101 = 96.0% 0110 = 96.2% 0111 = 96.4% 1000 = 96.6% 1001 = 96.8% 1010 = 97.0% 1011 = 97.2% 1100 = 97.4% 1101 = 97.6% 1110 = 97.8% 1111 = 98.0%	Health Check voltage threshold.

CONTROL4 - Control Register

Address = 0x21h	Default = 0xD7h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_LATCH_SPLMNT	BST_CLIM[1:0]		BST_VSET[4:0]				
Default	1	10		10111				
Access	R/W	R/W		R/W				

Name	Description		Notes
EN_LATCH_SPLMNT	0 = Allows IC to exit supplement mode if operating conditions allow 1 = Forces IC to stay in supplement mode until the STR voltage drops below BKIN_UV or VOUT drops below BUCK PG threshold		
BST_CLIM[1:0]	00 = 250mA 01 = 650mA 10 = 950mA 11 = 1500mA		Sets the boost convert peak switch current.
BST_VSET[4:0]	00000 = 5V 00001 = 5.6V 00010 = 7V 00011 = 8V 00100 = 9V 00101 = 10V 00110 = 11V 00111 = 12V 01000 = 13V 01001 = 14V 01010 = 15V 01011 = 16V 01100 = 17V 01101 = 18V 01110 = 19V 01111 = 20V	10000 = 21V 10001 = 22V 10010 = 23V 10011 = 24V 10100 = 25V 10101 = 26V 10110 = 27V 10111 = 28V 11000 = 29V 11001 = 30V 11010 = 31V 11011 = 32V 11100 = 33V 11101 = 34V 11110 = 35V 11111 = 36V	STR voltage set point

CONTROL5 - Control Register

Address = 0x22h	Default = N/A	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	"Reserved for factory use only"							
Default	"Reserved for factory use only"							
Access	R/W							

Name	Description	Notes
N/A	Reserved for factory use	Can be used as a scratch bit.

ADC_OFFSET – ADC Offset Register

Address = 0x23h	Default = N/A	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_OS[7:0]							
Default	N/A							
Access	R/W							

Name	Description	Notes
ADC_OS[7:0]	ADC offset data	Do not write to this register. Changing this register affects ADC read accuracy

ADC_GAIN – ADC Gain Register

Address = 0x24h	Default = N/A	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_GE[7:0]							
Default	N/A							
Access	R/W							

Name	Description	Notes
ADC_GE[7:0]	ADC gain error data	Do not write to this register. Changing this register affects ADC read accuracy

Buck1 – Buck Configuration Register

Address = 0x26h	Default = 0x0Bh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[3:0]				BK_DRVADJ[1:0]		BK_CLIM[1:0]	
Default	0000				10		11	
Access	R/W				R/W		R/W	

Name	Description	Notes
RFU[3:0]	Reserved for factory use	
BK_DRVADJ[1:0]	00 = 30ns / 15ns 01 = 20ns / 10ns 10 = 10ns / 6ns 11 = 5ns / 2.5ns	Adjusts the buck converter internal FET gate drive. These have been optimized by Active-Semi and should not be changed.
BK_CLIM[1:0]	00 = 5.0A 01 = 6.0A 10 = 7.0A 11 = 9.0A	Adjusts the buck converter's peak current limit value.

Buck2 – Buck Configuration Register

Address = 0x27h	Default = 0x70h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BK_SLP_ADJ[3:0]				SCALE_TSET_2X	SCALE_TSET_4X	SCALE_HCHK_2X	SCALE_HCHK_4X
Default	0111				0	0	0	0
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
BK_SLP_ADJ[3:0]	Buck slope compensation	Adjusts the buck converter internal slope compensation. This has been optimized by Active-Semi and should not be changed.
SCALE_TSET_2X	0 – Normal HMON_TSET 1 – HMON_TSET timing slowed by 2x	Need to explain what happens if bits 2 and 3 are = 11
SCALE_TSET_4X	0 – Normal HMON_TSET 1 – HMON_TSET timing slowed by 4x	Need to explain what happens if bits 2 and 3 are = 11
SCALE_HCHK_2X	0 – Health check performed every 4 minutes 1 – Health check performed every 8 minutes	Need to explain what happens if bits 0 and 1 are = 11
SCALE_HCHK_4X	0 – Health check performed every 4 minutes 1 – Health check performed every 16 minutes	Need to explain what happens if bits 0 and 1 are = 11

Buck3 – Buck Configuration Register

Address = 0x28h	Default = 0x60h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	BK_FREQ[2:0]			RFU[3:0]			
Default	0	110			0000			
Access	R/W	R/W			R/W			

Name	Description	Notes
RFU	Reserved for factory use	Always returns 0
BK_FREQ[2:0]	000 = 320 kHz 001 = 365 kHz 010 = 450 kHz 011 = 500 kHz 100 = 560 kHz 101 = 750 kHz 110 = 900 kHz 111 = 1130 kHz	Buck switching frequency in supplement mode.
RFU[0:3]	Reserved for factory use	Always returns 0

State_Machine – State Machine Register

Address = 0x38h	Default = 0x22h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	Mask_BKIN_nUV	Mask_eF_OC	Mask_eF_VIN_LT_VO	Mask_LDO_FAULT	Mask_STR_OV	Mask_STR_UV	Mask_BK_OV	Mask_BK_UV
Default	0	0	1	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
Mask_BKIN_nUV	0 – Normal operation 1 – Prevents IC from changing states when the buck input voltage (storage voltage) goes below 3.6V.	
Mask_eF_OC	0 – Normal operation 1 – Prevents IC from changing states when the eFuse goes overcurrent.	
Mask_eF_VIN_LT_VO	0 – Normal operation 1 – Prevents IC from changing states when VOUT – VIN > 120mV	
Mask_LDO_FAULT	0 – Normal operation 1 – Prevents IC from changing states when the LDO has a fault	
Mask_STR_OV	0 – Normal operation 1 – Prevents IC from changing states when the storage voltage goes over voltage.	
Mask_STR_UV	0 – Normal operation 1 – Prevents IC from changing states when the storage voltage goes under voltage.	
Mask_BK_OV	0 – Normal operation 1 – Prevents IC from changing states when the buck voltage goes over voltage.	
Mask_BK_UV	0 – Normal operation 1 – Prevents IC from changing states when the buck voltage goes under voltage.	

DEVICE ID – Device ID Register

Address = 0x3Bh	Default = 0x01h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DEVICE ID [7:0]							
Default	00000001							
Access	RO							

Name	Description	Notes
DEVICE ID [7:0]	8 bit word to identify the CMI in the IC. Refer to IC DS for Device IDs.	